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Simulation & Analysis of Sigma-Delta A/D Converter using VHDL-AMS

Prerna Gupta, Head & Prof. Rita Jain

Dept. of Electronics & Telecommunication Engg. LNCT Bhopal (M.P.) India

Abstract: Analog to digital converter is a fundamental component for digital processors since every signal which needs to be processed using digital algorithms requires the digital data. There are many different types of A/D converters are available but the sigma delta A/D converter has their unique advantage over others as they have only 10 to 15 percent analog components and rest are digital. This makes it good candidate when the A/D needs to integrate with the DSP in single chip, but the integration of two domains creates difficulty to evaluate the behavior of A/D using normal simulators hence special simulators called analog and mixed signal simulators are required in this paper we presented the detail simulation and analysis of sigma delta A/D using VHDL-AMS.

Keywords: sigma delta A/D Converters, VHDL-AMS.

1. Introduction

Signal processing is needed for almost every electronic system, & the techniques of processing can be broadly divided into two parts analog and digital, the analog systems are relative bulkier, less flexible and more sensitive to environmental conditions in the past they were the only possible choice because they don't need the complex processors and other related components which were difficult to manufacture at that time, but the advancements in chip manufacturing technology making it possible to design powerful processors on single chip and at cheaper cost. Nowadays the digital processing is preferred because it can overcome almost every problem faced by the analog processing.

The Digital Processing requires the signal in digital form hence for Digital Signal Processors needs internal or external A/D converters for external it could be of any type but for internal it is a totally different case because it requires compatibility with VLSI technology, in order to provide for monolithic integration of both the analog and digital sections on a single die. Since the Sigma Delta A/D converters are based on digital filtering techniques, almost 90% of the die is implemented in digital circuitry which enhances the prospect of compatibility [1].

2. Sigma Delta A/D Converter

This section describes the different technical terms and working of sigma delta A/D converter.

2.1 Sigma Delta Modulation

The work on sigma-delta modulation was developed as an extension to the well established delta modulation.

The arrangement shown in Figure 1 is called a Sigma-Delta Modulator [1]. This structure, besides being simpler, can be considered as being a "smoothed version" of a 1-bit delta modulator.

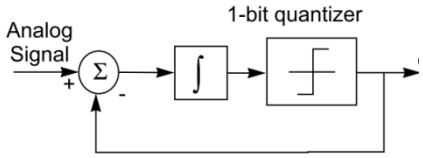

Figure 1: Sigma Delta A/D Modulator.

The name Sigma-Delta modulator comes from putting the integrator (sigma) in front of the delta modulator. The quantization noise like delta modulators, the S-D modulators use a simple coarse quantizer (comparator). However, unlike delta modulators, these systems encode the integral of the signal itself and thus their performance is insensitive to the rate of change of the signal.

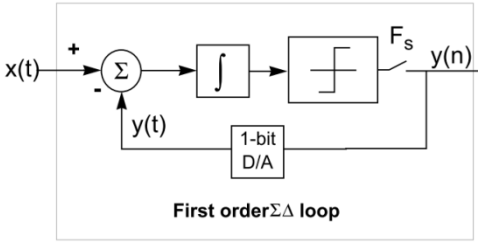

Figure 2: Sigma Delta A/D Modulator Practical Diagram.

2.2 Oversampling

The sigma delta A/D is an oversampling A/D converter because the signal is sampled at much higher than the Nyquist rate. The oversampling not only helps for tracking the original signal but also spreads the quantization noise over a larger band which helps in reducing the noise and designing of LPF the example can be considered as shown in figure.

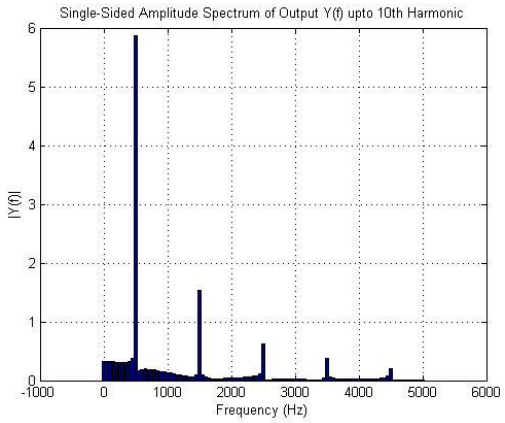

Figure 3: A sine wave of 500Hz is sampled at 1 Ks/s rate.

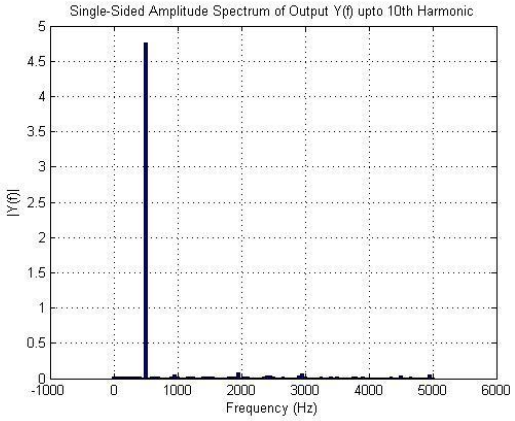

Figure 4: A sine wave of 500Hz is sampled at 100 Ks/s rate.

Now from figure 3 and 4 (without considering the harmonic distortion) it is clear that the noise floor at $2F_s$ sampling rate is about 0.25 and reduces to 0.05 at $100F_s$. It should be remember that the oversampling not reducing the total error energy but it distributes it over larger band.

2.3 Noise shaping

The noise shaping is a way of shaping the noise spectrum. In sigma delta A/D it is used to shift the

noise at spectrum at higher end. It is done by the integrator present in the forward path of converter.

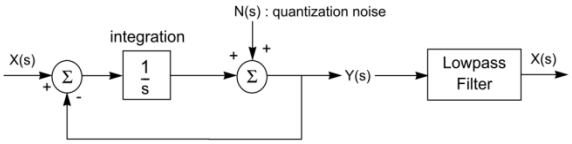

Figure 5: Descriptive Diagram of A/D converter.

The behavior of integrator as noise shaping element can better understand by figure 5 here the comparator is assumed as a noise producing element. Now the effect of integrator for both inputs X(s) and N(s) can be estimated by calculating the transfer function for each input separately.

Transfer function when looking from X(s) and considering N(s) = 0.

$$H_X(s) = \frac{\frac{1}{s}}{1+\frac{1}{s}} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (1)$$

The equation 1 can be simplified to

$$H_X(s) = \frac{1}{1+s} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (2)$$

This clearly shows the low-pass filter,

The transfer function when looking from N(s) and considering X(s) = 0.

$$H_N(s) = \frac{1}{1+\frac{1}{s}} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (3)$$

Simplifying the equation 3

$$H_N(s) = \frac{s}{1+s} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (4)$$

This is high-pass filter.

The equations (1) and (4) shows that the integrator acts differently for both and shifts the noise spectrum towards high frequency.

2.4 Decimation

The process of decimation is used in a sigma delta converter to eliminate redundant data at the output. The sampling theorem tells us that the sample rate only needs to be 2 times the input signal bandwidth in order to reliably reconstruct the input signal without distortion. However, the input signal was grossly oversampled by the sigma delta modulator in order to reduce the quantization noise. Therefore, there is redundant data that can be eliminated without introducing distortion to the conversion result [2].

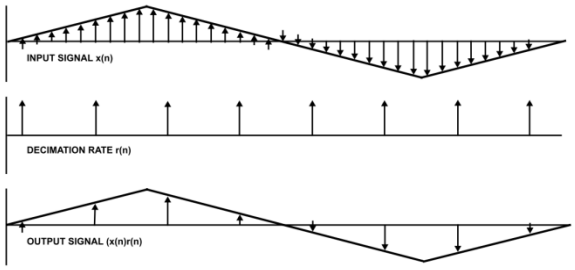

Figure 6: shows the decimation process by down sampling the original signal in time domain.

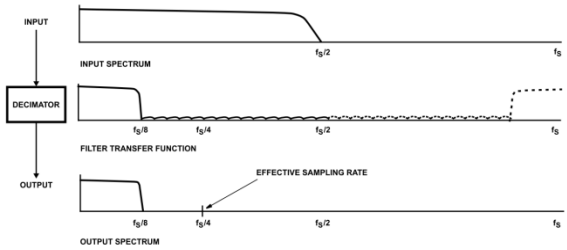

Figure 7: shows the decimation process in frequency domain.

3. Simulated Results & Analysis

The A/D model used in our simulation is given below

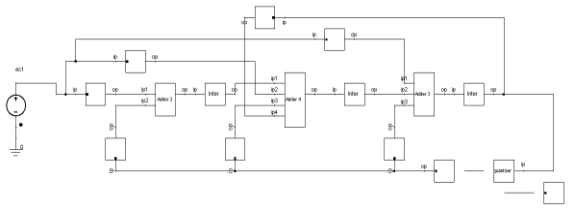

Figure 8: Simulated Model.

The figure describes a 3rd order sigma delta converter.

The above model is simulated for different sampling rates and two different input signal one is a sine wave of 500 Hz and other is ramp signal and the results are as below.

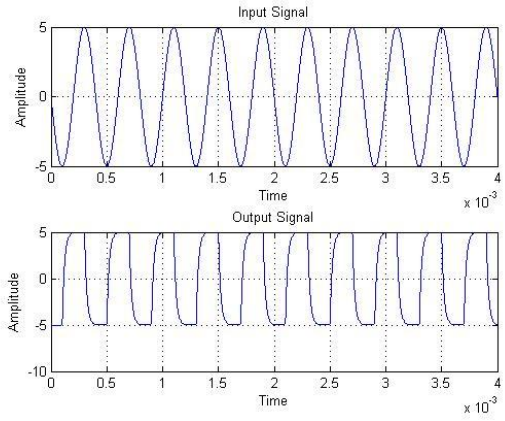

Figure 9: Input and output waveform when sampled at $2F_s$ rate.

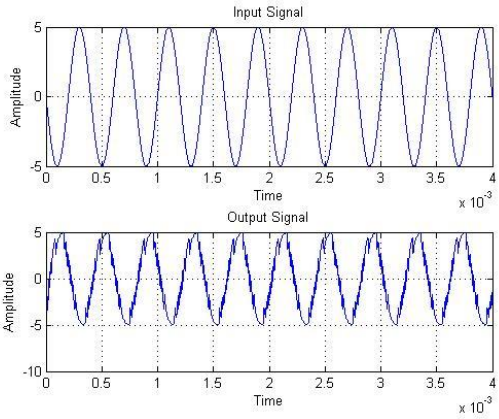

Figure 10: Input and output waveform when sampled at $100F_s$ rate.

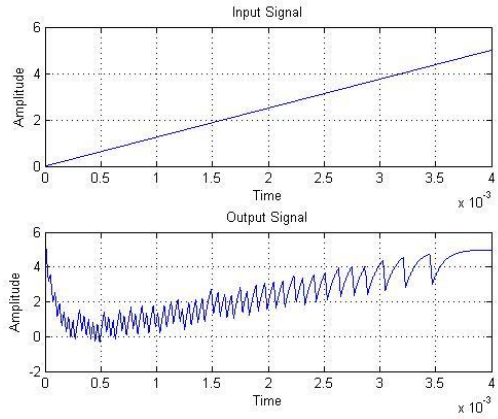

Figure 11: Input and output waveform when sampled at $50F_s$ rate.

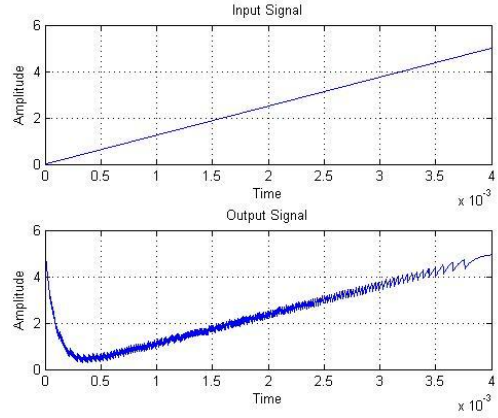

Figure 10: Input and output waveform when sampled at $100F_s$ rate.

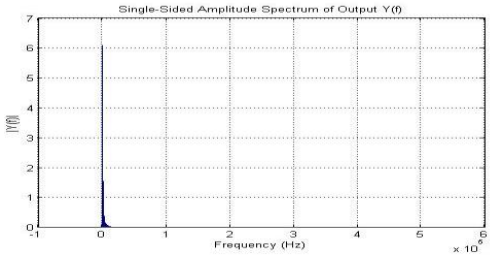

Figure 12: Spectrum plot of output signal for sine wave sampled at $2F_s$.

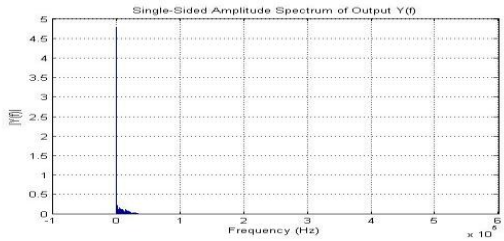

Figure 13: Spectrum plot of output signal for sine wave sampled at $100F_s$.

Table 1: Results in tabulated form

Fs	ENOB	THD	SINAD	SNR	INL
1000	0.51	-11.75	10.75	81.39	80.53
2000	0.97	-10.75	10.75	80.39	80.77
5000	-1.01	-11.24	-4.32	-2.74	70.89
10000	0.473	-4.6	4.60	73.38	65.56
20000	0.85	-6.8989	6.89	67.62	44.23
50000	1.83	-13.19	12.81	40.15	23.12
100000	2.509	-17.68	16.86	37.76	12.43
500000	4.44	-32.56	28.49	37.03	4.44

Following are the abbreviations used in table.
F_s = Sampling Frequency in Hz.
ENOB = Effective Number of bits.
THD = Total Harmonic Distortion (in dB).
SINAD = Signal to Noise and Distortion Ratio in dB.
INL = Integral Non Linearity in %.

4. Conclusion

The simulation has been performed using VHDL-AMS because we don't have any physical device equivalent to the model it could not be cross checked but the simulated results are close to the theoretical results and hence it can be said that the simulation results are close to real and according to simulated results following conclusions can be drawn the effective number of bits for 1 bit A/D can be increased by oversampling, the THD, SINAD, SNR, INL greatly improves with sampling rate. We can also say that VHDL-AMS provides great ease and facility for modeling the mixed signal models with proper accuracy.

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