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Noise Tolerance Enhancement with Leakage Current Reduction in Dynamic Logic Circiuts

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***Abstract*—To improve noise tolerance of the dynamic logic circuits with leakage current reduction , a new noise tolerant technique is proposed here. Average noise threshold energy (ANTE) metric is used to compare the noise tolerance ability of the existing techniques with the proposed technique. A two input AND gate is designed and simulated using 0.18 micron technology and at a clock frequency of 100MHz. Simulation results indicate that the proposed technique provides an improvement of 77.72% in ANTE with a reduction of leakage current by 73.9% over the conventional domino technique.**

***Keywords*— ANTE, Noise Tolerance, Dynamic Circuits, crosstalk, power consumption.**

I. INTRODUCTION

Dynamic CMOS logic circuits are used in high performance VLSI chips in order to achieve very high system performance. Noise is a major issue in design of dynamic CMOS logic circuits. In deep submicron region noise tolerance of dynamic CMOS logic circuit is very poor and they are more prone to logic failure.

Dynamic circuits offer compactness, higher speed as compared to static CMOS circuits. However aggressive scaling of device and interconnect dimensions, power supplies in deep submicron region have further degraded the reliability of dynamic circuits. Noise is digital integrated circuits refers to any phenomenon that causes the voltage at a node to deviate from its nominal value [1]. Noise phenomena always existed and they had an impact on the performance of dynamic circuits but it is technology scaling that has made the noise effects much more severe. In deep submicron region various noise sources are related to cross talk, leakage current, charge sharing and variations in the supply voltage. Leakage current increases exponentially with the scaling of device dimensions.

Dynamic logic circuits are much affected by noise as compared to static CMOS circuit. This is due to the fact that dynamic logic circuits have lower value of switching threshold voltage, which is equal to the threshold voltage of the pull down NMOS devices. On the other hand, switching threshold voltage of static CMOS logic circuit is around half the supply voltage.

In past two decades a number of techniques have been developed to improve noise tolerance of dynamic circuits but they improve the noise tolerance at the cost of other important design metrics like speed, power consumption, circuit area.

In this paper we propose a technique that enhances the noise immunity of the dynamic circuit without compromising much on other important design metrics. To prove the efficiency of proposed technique, a 2 input AND gate has been designed with 180nm – 1.8 V CMOS process. This paper is organized as follows: In section II various noise sources and their effect on the performance of dynamic logic circuits are described. Section III presents an overview of existing technique for improving the noise tolerance of dynamic logic circuits. Proposed noise tolerant design technique is described in section IV.

Section V describes the metrics used for analyzing the proposed technique and simulation results are presented and finally in section VI conclusion are drawn.

II. NOISE PROBLEM IN DEEP SUBMICRON REGION

Fig.1 shows a two input domino AND gate. Two major phases of operation of this circuit are precharge and evaluation. During precharge phase CK = 0, output node S is precharged to V_{DD} as M1 is on. MP is off during precharge phase & pull down path is disabled.

During evaluation phase CK = 1, M1 is off & M4 is on. So output node is conditionally discharge based on the input values.

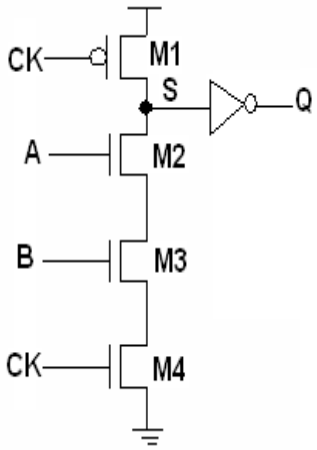


Fig. 1 Two-input Domino AND gate.

Various noise source in dynamic logic circuits are charge sharing noise, leakage noise, crosstalk noise, power &ground noise, substrate noise. Charge sharing can occur when clock makes transition i.e. CK = 1, charge is redistributed between the dynamic node and the internal nodes of the pull down network. Charge sharing reduces the output voltage & can cause false switching of a dynamic logic gate.

Leakage noise is caused by the high impedance state of the output node during the evaluation mode when the pull down path is turn off. Due to aggressive scaling of inter connect lateral dimensions with relatively unchanged vertical

dimensions cross talk noise has become a major source of failure for deep submicron VLSI circuits. Parasitic resistance and inductance at the power and ground network and at the chip package are the cause for power and ground noise. Threshold voltage of MOS depends on the substrate voltage and hence noise in the substrate can lower the threshold voltage of transistors in the pull down network, thereby making it much more susceptible to noise.

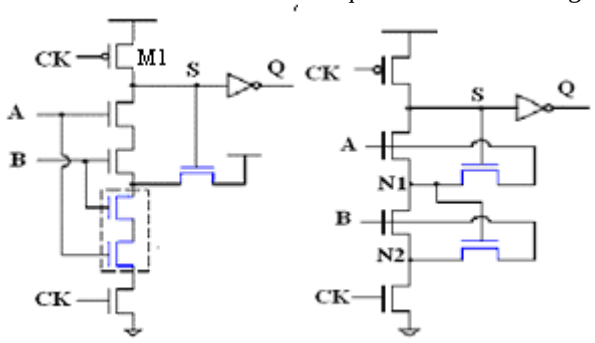
Above discussed noise sources along with other sources of noise affect the reliability of dynamic logic circuit in deep submicron region and so a noise tolerant design technique is required which can improve the noise tolerance of a dynamic logic circuit against all types of noises in the deep submicron region.

III. OVERVIEW OF THE EXISTING NOISE TOLERANT DYNAMIC CIRCUIT DESIGN TECHNIQUES

A number of circuit techniques have been proposed to improve the noise tolerance of dynamic logic circuit in deep submicron region. In this section there techniques namely – Mirror Technique, Twin Transistor technique, Triple Transistor technique are described.

Fig.2(a) shows a 2 input AND gate implemented using Mirror Technique.Mirror technique employs a feedback controlled NMOS transistor. It also duplicates the pull down network to reduce dc power consumption and to further improve gate noise tolerance. Operation of this circuit is based on the principle of Schmitt trigger. During precharge phase CK = 0, M1 turns on & hence node S is charged to logic high. Assuming that node S is initially discharged, then node S reaches the value of (V_{DD} – V_{th}). Due to body effect, the switching threshold voltage of top NMOS net is increased thereby increasing the noise immunity.

Twin Transistor technique is illustrated in fig.2(b).



(a) (b)

Fig.2 (a) Mirror Technique (b) Twin Transistor Technique.

In this circuit additional transistor called twin transistor increases the turn on voltage of the pull-down network by pulling up the voltage of the common – source node.

Fig.3 shows triple transistor technique.

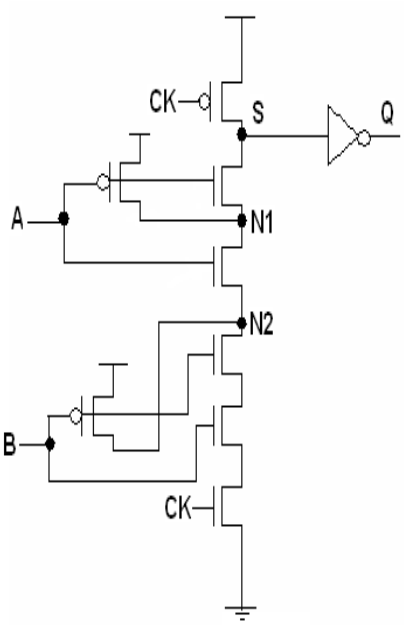


Fig.3 Triple Transistor Technique.

In this technique more transistors are added to N – logic to improve the noise tolerance. PMOS transistor rises the voltage of N1 & N2 to V_{DD} while the gate input are low. Additional NMOS transistor is used to prevent the possible dc conducting path problem in the evaluation phase [1]. All the three technique discussed so far suffer from some or other performance loss i.e. in terms of area overhead, power consumption & speed.

Twin transistor technique is not suitable for certain logic functions because it may short input nodes & hence will produce erroneous results. Mirror technique and Triple transistor technique increase the length of gate discharge path. So there is a need to develop noise tolerant technique that should have: minimal area overhead, minimal speed overhead, improves gate noise tolerance against all types of noise, should be suitable for all logic functions and should have minimal power consumption overhead.

IV. PROPOSED TECHNIQUE

Fig.4 shows the schematic diagram of the proposed noise tolerant technique. It basically consists of 7 parts:

(a)Transistor M2 is the pre-charging transistor.
(b)Transistor M3 is used as a stacking transistor.
(c)Transistor M6 is used as a delayed clocked transistor.
(d)Pull-down Network (PDN) defines the logical functionality of the circuit.
(e)Inverter is used for providing Domino functionality.
(f) M1 and M7 are sleep transistors which are incorporated to reduce the standby leakage power.
(g) Transistor M8 is used as source potential raising transistor.

Control logic provides two clocks namely CK and DCK. DCK is generated by delaying the clock CK using a delay circuitry, which can be made using chain of inverters.

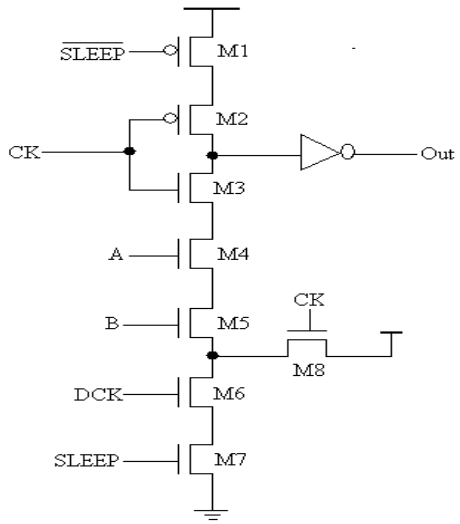


Fig.4 Proposed Technique

A. Noise-tolerance mechanism of the proposed technique:-

By raising the source voltage: In order to increase the noise immunity of the circuit against the external noises (mainly the coupling noises) arriving at the inputs of the pull down network, it is imperative that the threshold voltage of the PDN transistors increases. The commonly used technique of improving the threshold voltage is to increase the source voltage of the respective transistors. Since the gate voltage has to be greater than the sum of the source voltage and the transistor threshold voltage when a transistor is turned on, higher source voltage directly leads to increased gate turn on voltage. Furthermore, due to the body effect, transistor threshold voltage is increased when the source voltage rises. This also contributes to improving gate turn-on voltage. Here NMOS transistor M8 is used to raise the source potential of the pull down network. But instead of loading the output by taking feedback as in Mirror Technique, here the clock is used to drive the source raising transistor. This causes the source body biasing voltage to increase, resulting in increase of the threshold voltage of the transistor. Thus the PDN can now sustain more amount of noise arriving at the gate input.

Stacking: The proposed technique relies on reducing the sub threshold leakage current to increase wide fan-in domino circuit's noise immunity; this leakage current is one of the main sources of noise in dynamic circuits. To reduce the sub threshold leakage we make use of the stacking effect which indicates that the sub threshold leakage of a stack of two transistors is reduced if both transistors are OFF. Charge sharing problem is also somewhat reduced as the path to the PDN remains closed during the pre-charge phase because of M3.

Feeding trasistor M6 with delayed clock:
During the evaluation phase and stage II as shown in Fig.5 the CK signal is high which turns on the transistor M3. However as the DCK signal is still low the transistor M6 remains off. This shuts down the path between the dynamic node and ground. So even if a coupling noise arriving at the input terminals turn on the PDN transistors, the dynamic node n1 may not get completely discharged, depending on the noise pulse duration. During this isolation leakage noise is further reduced due to the stacking effect imposed by the transistor M3 and the PDN transistor. The noise immunity is indeed improved because any noise influence at the circuit inputs for that short duration is not reflected at the node n1 and at the output.

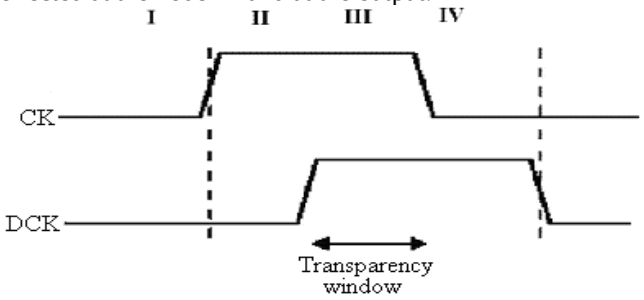


Fig.5 Noise Tolerance Mechanism

Leakage current reduction using sleep transistors(M1 & M7):
In the active state both the sleep transistors M1 and M7 are on and the circuit functions as usual. In the standby state, both the transistors are in the off state and this disconects the gate from the ground.To guarantee the proper functionality of the circuit, the sleep transistor has to be carefully sized to decrease its voltage drop while it is on. Since leakage current is one of the main sources of noise in dynamic circuits, its reduction in both the standby and active mode of operation of the circuit would mean the improvement in the noise tolerance.

V. SIMULATION RESULTS

A two input AND gate is designed using the proposed technique. A noise injection circuit (NIC) is used to apply noise pulses of certain amplitude and duration to one of the inputs of the two input AND gate. Simulations were done with Tanner SPICE version 13.0 simulator and transistor models of 0.18 micron process technology . The proposed technique is compared with Domino techcique, Twin transistor technique, Triple transistor technique and Mirror technique.The parameters used for comparision are leakage current, power consumption, ANTE (Average Noise Threshold Energy).

ANTE is defined by-

$ANTE = E (Vn^2.Tn)$

Where Vn is the noise amplitude and Tn is the noise width that causes the gate output to switch. E() denotes the average value.

Fig.6 shows the noise immunity curves for two input AND gate. It is quite clear from the graph that for larger noise pulse width the proposed technique and Mirror technique have comparable noise immunity but for a given noise pulse width, the proposed technique is gving much better noise immunity than other techniques.

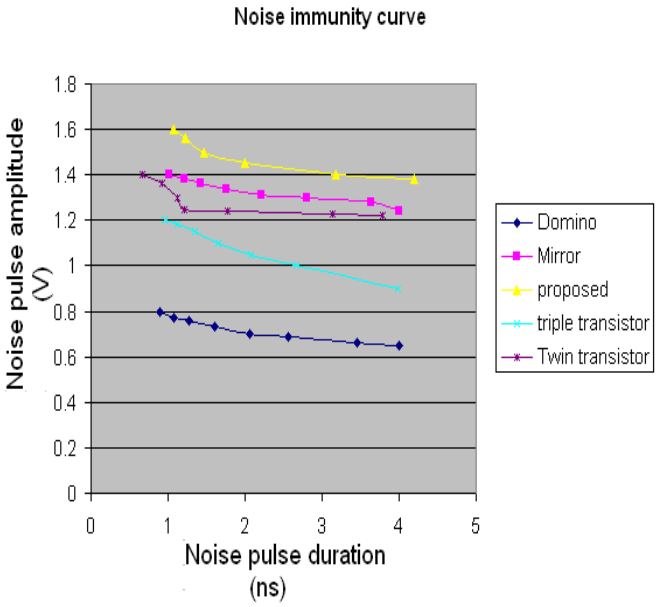


Fig. 6 Noise immunity curves for two input AND gate.

Fig.7 shows the Noise Threshold Energy curves for the two input AND gate. A larger value of *NTE* measure implies that a higher noise pulse amplitude V, or equivalently larger noise energy is needed to discharge the dynamic node and cause a logic error. The proposed technique exhibits higher NTE value as compared to other techniques and it shows that it is more tolerant to noise.

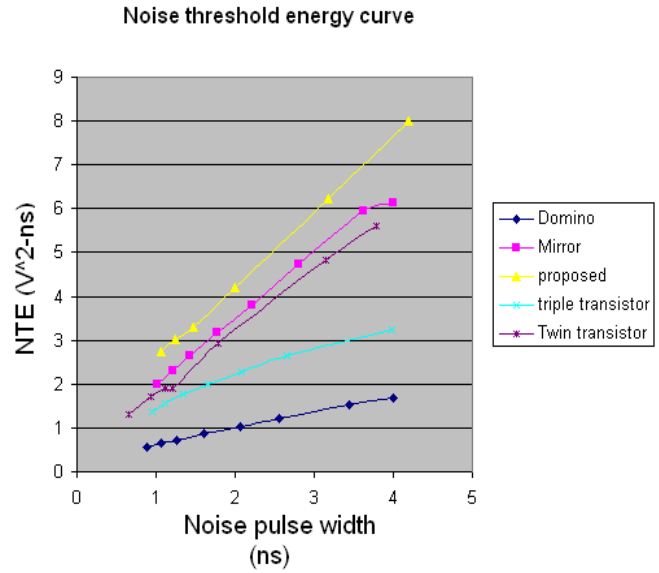


Fig.7 Noise Threshold Energy curves for tow input AND gate.

Fig.8 shows the variation of noise immunity with power supply.

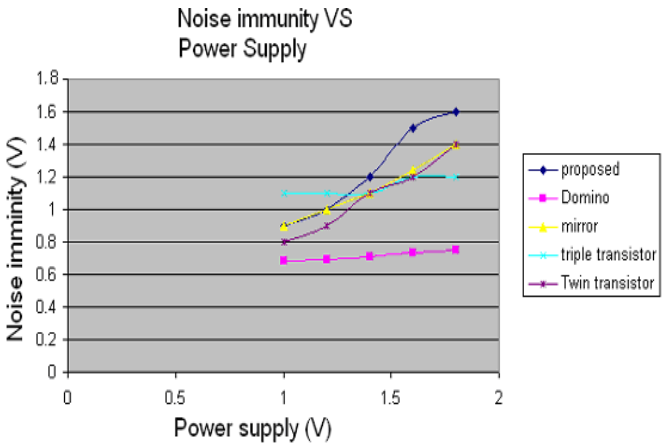


Fig.8 Noise immunity Versus Power Supply.

The proposed technique increases noise immunity by 53% as compared to Domino technique, 25% as compared to Triple transistor technique, 12.5% as compared to Twin transistor and Mirror technique.

The bar chart in fig.9 shows that the values of ANTE for different techniques at 1.8V. At 180nm technology, proposed technique improves ANTE by 77.72% as compared to domino technique, 16.15% as compared to miror technique, 37.11% as compared to twin transistor technique, 53.71% as compared to triple transistor technique.

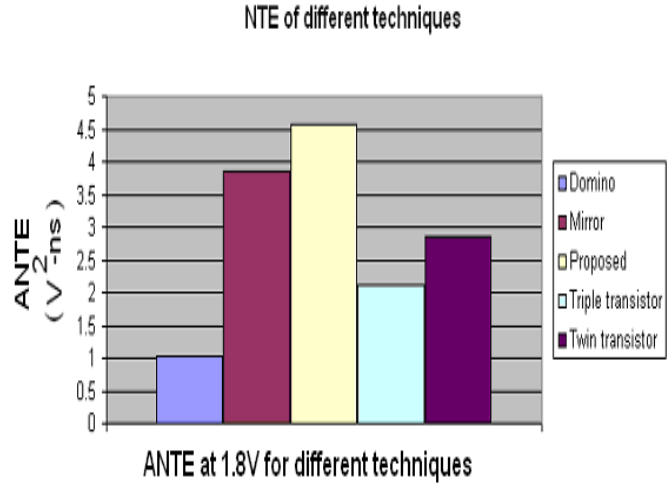


Fig.9 ANTE values at 1.8V for different techniques.

The chart in fig.10 shows the values of leakage current at 1.8V. The proposed technique's leakage current is 73.9% less than the domino technique, 50.46% less than twin transistor technique, 44.61% less than triple transistor technique.
Mirror technique's performance is slightly better than the proposed technique as far as leakage current is concerned. Mirror technique has 29% less leakage current as compared to the proposed technique.

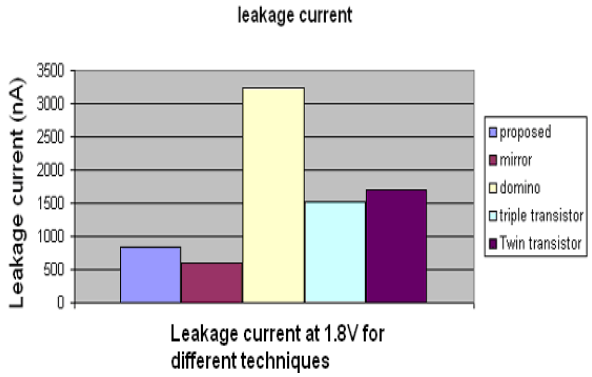


Fig.10 Leakage current values at 1.8V for different techniques

The chart in fig.11 shows the values of Average power consumption for different techniques at 1.8V.

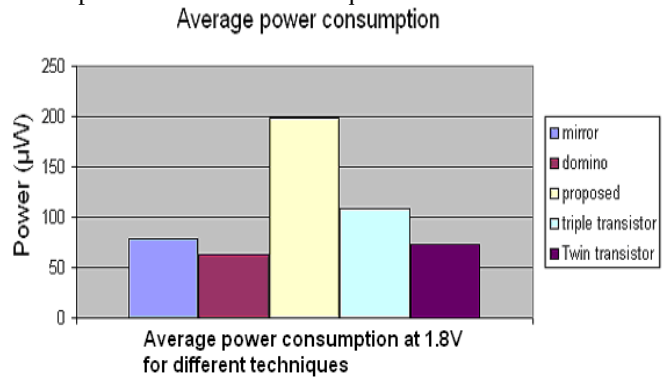


Fig.11 Average Power Consumption at 1.8V for different techniques

proposed technique consumes 45.52% more power as compared to the triple transistor technique. Domino technique is showing the lowest power consumption. It consumes around 63.85% less power as compared to the proposed technique and hence is most power efficient as compared to all the techniques. Twin transistor technique and mirror technique consumes around 14.2% and 20.2% more power respectively as compared to the domino technique.

TABLE I
PERFORMANCE COMPARISION FOR 2 INPUT AND GATE

Technique	Average Power Consumption (µW)	ANTE (V^2ns)	Leakage current (pA)
Domino	63.006	1.02	3.24
Mirror	79.007	3.84	0.599
Triple Transistor	108.47	2.12	1.524
Twin Transistor	73.516	2.88	1.704
Proposed	199.13	4.58	0.844

The proposed technique requires less number of transistors for implementation of large fan-in circuits as compared to other noise tolerant techniques.

VI. CONCLUSION

The feasability of the proposed noise tolerant dynamic circuit technique has been shown by means of simulation and experimental results. The proposed technique exhibits high noise immunity and is adequate for designing large fan-in gates . As already shown in the simulation, the proposed technique gives 77.72% improvement in ANTE over domino technique, but this improvement in ANTE is achieved at the cost of higher power consumption and future work will be directed towards using low power designing techniques so that both improvement in the noise tolerance and power consumption can be achieved at the same time.

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