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A survey of Design Technologies for LowPower VLSI System

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Abstract

Power is most important t factor in any system design. The need for low power has caused a major factor where power dissipationhas become as important a consideration as performance and their area. Thispaper reviews various strategies and methodologies for designing low power circuitsandsystems. Thispaperexplains the connection between scaling and power consumption and design robustness. The paper concludes with future challenges that must be met to design low power high performance systems.

Key word: PSSL,DS-PSSL,BTBT,DPSCRFF.

INTRODUCTION

In past, majorconcern in front of designer was area, performance cost and reliability [1] power consideration was mostly of only secondary importance. In recent year through vlsi technology these problem were overcome by scaling large circuits into small.This, however, has led to exponential increases in power consumption that has reached the limits of reliability. In addition, the continue scaling into the nanometer, the problem of robustness such as-signal integrity and soft error has to face to designers.Furthermore,
the issues of power consumption and robustness only get worse with time. How the low power consumes in system design with small area is the most researching subjectfor designers.

At the circuit level, choice of logic style is important because it directly affect power, performance and robustness. There are generally two logic styles static CMOS and domino logic[2].Static CMOS is too slow to be used in timing-critical designs but it is energy efficient and robust. Domino logic, though fast, consumes too much power and is not robust.So we required new digital logic techniques and style that are simultaneously energy efficient, robust to noise and high performance.

PSSL (preset skewed static logic) is a new family of logic style. PSSL is better than domino in term of robustness and energy, and is generally better than static CMOS in term of delay. PSSL works byPartially overlapping. The execution of consecutive iterations through speculative evaluation. This is accomplished by presetting nodes at register boundaries before input arrival. Thiscreates timing slack which can be traded for lower delay and/or lower energy. We alsoshow a leakage reduction technique in PSSL that takes advantage of this slack to reduce-energy-delay overhead.

SOURCE OF POWER DISSIPATION

In logic design, chip power can be divided into two main component dynamic switching and static leakage. Dynamic power dissipation ignore short circuit current which is a small fraction of total dynamic power, is given by P=1/2CV^2f. WhereC=average on chip capacitance switched per cycle.V=supply voltage.

The reduction in oxide thickness [4] and threshold voltage has led exponential increase in static leakage power.Static Power dissipation in CMOS circuit is caused by three sources of leakages:1)sub threshold leakage 2)gate leakage 3)band-to- band tunnelling(BTBT) leakage .Sub-threshold leakage is the current flowing between source to drain(or drain to source) when transistor is nominally off. Gate leakage is the current flowing from gate to source or drain. This is caused by direct tunneling of holes or electrons through oxide insulator. BTBT is the current flowing from reverse bias of drain-substart or source-substartjunction. In these components sub threshold leakage was major component in all leakage at technology larger than 130nm [5]. So there are a trade off relation between static and dynamic power consumption.From the above formula we can say that power dissipation is depend on physical capacitance, so, in addition to operating at low voltages, minimizing capacitances offers another technique for minimizing power consumption. With this understanding, we can now consider how to reduce physical capacitance. Capacitance can be kept minimum by using less logic, smaller devices, fewer and shorter wires. So capacitance can be reducing by reducing size of devices, but it also reduces current of transistor which makes its operation slow.

LOGIC STYLE

There two most common basic logic styles are static CMOS and domino. A static CMOS logic network is composed of two networks: a pull up network, consisting of PMOS transistor which is connected to power and a pull down network, consisting of NMOS transistor, which is connected to ground. The networks are constructed such that only one network conduct at a particular time in the given set of input.Static CMOS is a universal logic – any logic function can be implemented.The logic design of static CMOS is very simple, there are no clocks and no feedback involved in static CMOS, also the gates are generally relatively easy to lay out. This simplicity of static CMOS generally leads to relatively low power dissipation, especially for low fan-in gates.

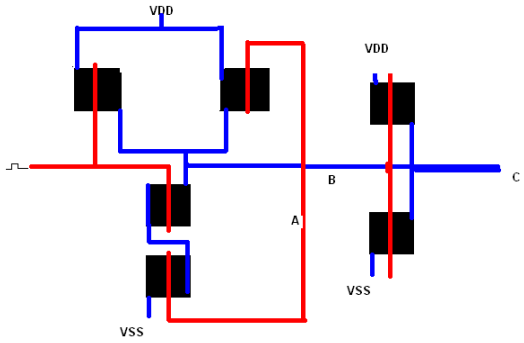
The problem with static CMOS is that it performs too poorly for the most aggressive designs. CMOS always required at least two transistor per input that is-pull up and pull down.In addition, it is not very efficient in implementing circuitssuch as XOR/XNOR, wide-fanin NOR, or binary encoded multiplexers, requiring an exponentialnumber of transistors and/or a n transistor pull-up chain for n inputs.A domino logic network composed of alternating dynamic and static CMOS gates. In dynamic gate, the PMOS pull up chain of static CMOS gate is replaced with a clocked pull up transistor, which reduce input load by factor of 1+r, where r is the PMOS to NMOS width ratio. If the input clock is low, output node is precharged high and when the input clock rises, the gate evaluates, conditionally discharging the dynamic node.Domino logic frequently used in high speed design because of the higher performance of dynamic gate.
A dynamic logic gate generally differs from the equivalent static CMOS logic gate because the logical effort for each gate is lower.

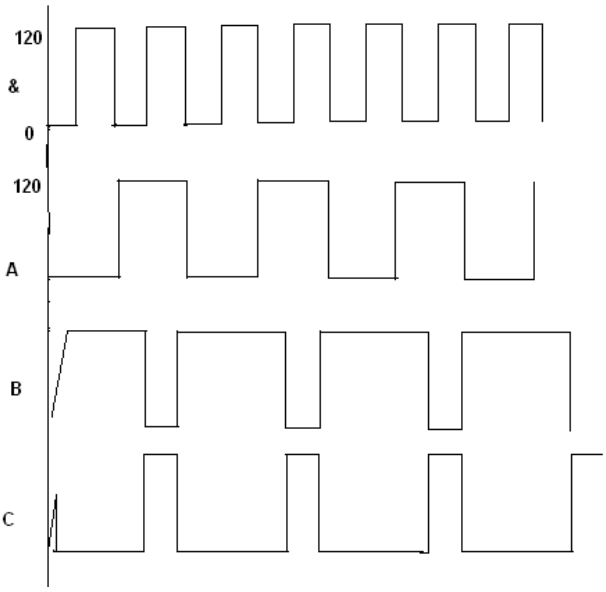
Gate type	Static	Footed dynamic	Footless dynamic
	Logical effort	Logical effort	Logical effort
INV	1	2/3	1/3
NAND	(N+2)/3	(N+1)/3	N/3
NOR	(1+2N/3)	2/3	1/3
One hot MUX	2	1	2/3
SymmetricXOR	N2^(N-1)	N/A	N/A

Where n is number of inputs. Theratio of NMOS to PMOS drive is assumed to be 2. Static gates are sized to have balancedrise or fall delay.The performance of domino logic comes at the cost of power, robustness, and designeffort. Domino logic consumes more power because number of transistor increased in output.

PRESET SKEWED STATIC LOGIC

Skewed static logic is a chain of static CMOS inverter. More generally it is a multiple- input, multiple output acyclic combinational circuit, which has many activation paths. If there are any differences in delay times between different paths, than there is a slack.By appropriately resizing transistors, one can often use slack to either increase performance or reduce power dissipation. A simple PSSL circuit resembles the chain of static inverters except that the first inverter has been replaced by NAND gate in which clock is tied in one input. The logical function of this circuit is the same as the inverter chain. PSSL combines the energy efficiency and robustness of static CMOS logic with the





Performance of domino logic.Let us assume that the input A is expected to arrive at the rising edge of theclock. First, the

falling edges of clock initiate the process of preset. In this time all circuit nodes are indirectly forced to pre-determined values. In particular, node B rises in turn causing node C to fall.The idea behind the preset process is that we are computing all the nodes ofthe circuit presuming low input values. This begins one clock phase before the actual inputvalue(s) arrive, so this computation has an extra clock phase to complete.

The rising edge of the clock initiates the process of evaluate. The process of evaluate is independent of the process of preset, and, in particular, evaluate can begin before preset completes. If the value of the input node, A is low at the rising edge of the clock and remains low, nothing further happens in the circuit and evaluate is complete.However, if the input node, A, is high when the clock rises or node A rises while the clock is high, then it causes node B to fall, in turn causing node C to rise, completing the evaluateprocess.Whether node A is high or low, eventually node C gets the correct value. However, we have decoupled the computation for low values of A (the preset process) from the computation for high values of A (the evaluate process), giving the former computation extra timeand thus creating slack in the path of transistors in the preset process (i.e. the preset path).We can take advantage of this slack by reducing the size of transistors in the preset pathto reduce power consumption, or by increasing the size of transistors in the evaluate pathto reduce delay. Preset allows PSSL to outperform generic static CMOS logic. However preset comes at the cost of extra power consumption because of spurious transitions from input mis-speculation and extra clocking overhead.

PIPELINING

Now we create pipelining using PSSL. PSSL using three major clocking schemes: level sensitive, edge trigger and pulsed.Level-sensitive clocking uses alternating transparent latches as timing elements. A two phase Level-sensitive (LS-PSSL) pipeline is the composition of PSSL pipeline stages of alternating phase, separated by transparent latches.In LS-PSSL, the transparent latchesserve two purposes. First, they hold pipeline state. Every legal pipeline must have at least one latch in each full pipeline stage. Second, the latches preventthe preset wave-front from propagating to the following stage until after the preset phase. Every legal pipeline must have a total of exactly one cycle ofdelay in each full pipeline stage. It is possible to extend LS-PSSL to arbitrary numbers of clock phases.

In edge trigger clocking only single monolithic timing element (flip flop) is use.Pulsed clocking uses transparent latches that are clocked with narrow pulses It uses a novel flip-flop structure which is call the Double Pulsed Set Conditional-Reset Flip Flop (DPSCRFF). In DPSCRFF, the path from input to output is only single stage of logic, so it givehigh performance.Another advantage is that the data input sees only a single transistor load which reduces required input drive and energy consumption.Pulsed-PSSL, Edge-triggered PSSL, and LS-PSSL make use of wave pipelining. This technique, however, becomes harder to use in the face of variability. So we should be careful to analysis of minimum clock width constraints.This only becomes a problem if there is no clock frequency that simultaneously satisfies minimum clock width constraints on the fast corners and maximum clock width constraints on the slow corners.

CONCLUSION

There is not likely to be a single logic element which satisfies all best condition for logic design.Static CMOS logic and Domino logic occupy very different points in the energy-delayrobustness space. Static CMOS is good in terms of energy and robustness, but is poor in terms of delay. Domino is good in terms of delay, but is poor in terms of energy andHowever we believe on PSSL complements and can improve logic styles and timing elements.It achieves higher performance, lower energy, and higher robustness It is also easier to design and widely applicable. In figure circuit and wave form of input and output is shown.

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