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Design of Low Voltage and Low Power D-Flip Flop

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***Abstract*— This paper presents a novel D flip-flop for low voltage operation with improved speed using SPICE simulation, it takes advantage of a dynamic threshold voltage using DTMOS for ultra-low voltage operation and a negative differential resistance storage using Bistable Gated Bipolar Device (BGB). DTMOS provides low power consumption and BGB provides high speed because of less capacitance. So we have taken advantages of both the DTMOS and BGB device to make the D-Flip Flop for low power operation with high speed and low leakage current. Leakage is further reduced by addition of two sleep transistors.**

***Keywords*— BGB, DTMOS, CMOS and sleep Transistor.**

I. INTRODUCTION

The design of high-density chips in MOS Very Large Scale Integration (VLSI) technology requires that the packing density of MOSFETs used in the circuits is as high as possible for that sizes of the transistors should be as small as possible. The reduction of the size, i.e., the dimensions of MOSFETs, is commonly referred to as *scaling*. Scaling of supply voltage (V_{DD}) is also an effective method to reduce the dynamic power (P_d) in CMOS digital circuits because the dynamic power is directly proportional to the square of supply voltage. Scaling down of threshold voltage ideally causes the leakage current per transistor to increase by five times per technology generation. However, the threshold voltage (V_{th}) reduction leads to exponential increase of subthreshold leakage, which is a major challenge for low voltage digital design. The multi V_{th} technique is an approach for most digital circuits to reduce sub threshold leakage current. A dynamic threshold voltage MOSFET (DTMOS) is promising for ultra-low V_{DD} (0.6 V and below) which provides high V_{th} for low off-state leakage and low for high on-state current drive. On the other hand, negative differential resistance (NDR) devices provide high-speed storage because of less capacitance. The above advantages of DTMOS and NDR devices can be used to make D flip-flop. In this paper, we propose such a novel D flip-flop (DFF) using the bistable gated bipolar (BGB) device as an NDR device.

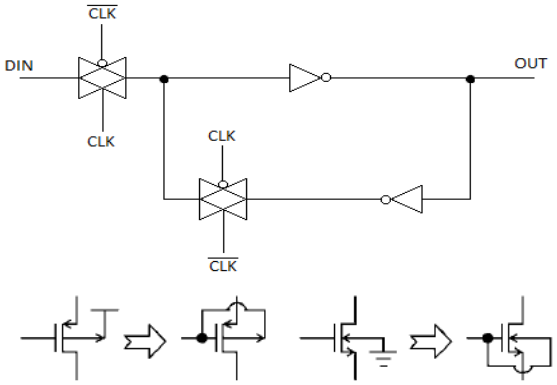
II. LATCH DESIGN

Latches and flip-flops are the basic elements for storing information. One latch or flip-flop can store one bit of information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted.

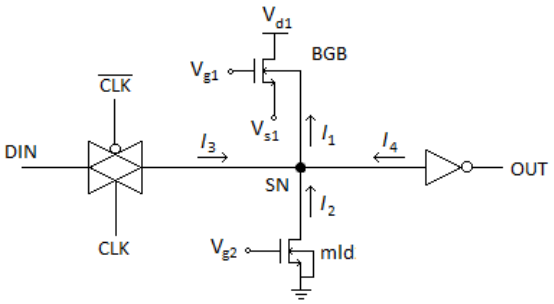
In other word, when they are enabled, their content changes immediately when their inputs change.

Flip-flop on the other hand, have their content change only their at the rising or falling edge of enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop contents remain constant even if the input changes.

In this work we design CMOS latch, CMOS-BGB latch, DTMOD latch and DTMOS-BGB latch.

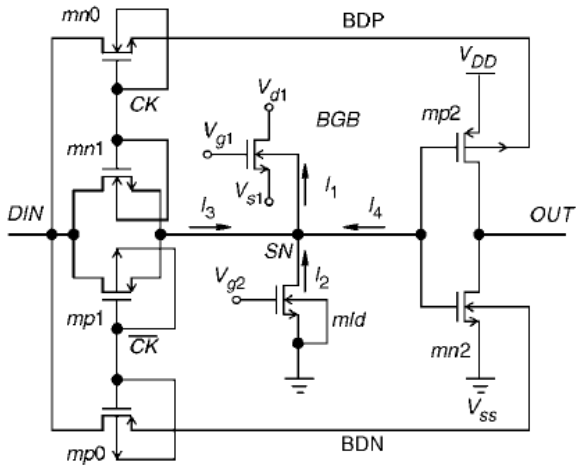


(a)



(b)

$V_{d1} = 3.5$ V, $V_{g1} = 1.8$ V, $V_{s1} = 1.5$ V, $V_{g2} = 1$



(c)

$V_{d1} = 2.0\ V,\ V_{g1} = 0.5\ V,\ V_{s1} = 0.7\ V,\ V_{g2} = 0.53\ V$

Fig. 1 Schematics of different static latches,
(a) CMOS latch,
(b) BGB latch and
(c) DTMOS-BGB latch.

A DTMOS latch can be designed by replacing each MOSFET in CMOS latch by connecting body terminal of transistor to its gate terminal. This methodology can be applied to a CMOS latch to form a DTMOS latch as shown in fig 1(a). To design BGB latch, it is difficult to replace all MOSFETs in a CMOS NDR latch[2]. So we replaced only pass gate in CMOS NDR latch but not to the inverter in that the large body currents through the forward biased body-source junctions will increase I4 in magnitude and lead to malfunction of the BGB storage cell. This problem can be solved, as shown in Fig. 1(c), by connecting the body nodes (BDN, BDP) of the inverter MOSFETs (mn2 and mp2) to DIN through a proper DTMOS pass gate, respectively, i.e. a p-channel DTMOS (mp0) to pull BDN high and an n-channel DTMOS (mn0) to pull BDP low. When the pass gates are on (CLK=1), the inverter MOSFETs (mn2 and mp2) act as DTMOS with their gates and bodies equal to DIN. When the pass gates are off (CLK=0), the storage node (SN) is separated from BDN and BDP so that the charge on it can be held with the BGB storage cell by impact ionization, without which it will leak away with time. Meanwhile, each body voltage (V_B) of mn2 and mp2 is approaching a stable point close to its source voltage owing to its body-source diode current compensated by the source leakage of mp0 or mn0, eventually making a high-V_{th} inverter.

III. PROPOSED TECHNIQUE

In proposed work we used BGB-DTMOS technique along with the sleep transistors in the output inverter in order to reduce the leakage power dissipation in the standby mode.

This technique is very effective and easy to implement in CMOS based circuits as the reduction in the leakage power is obtained by the addition of only two transistors and hence area overhead is also less.

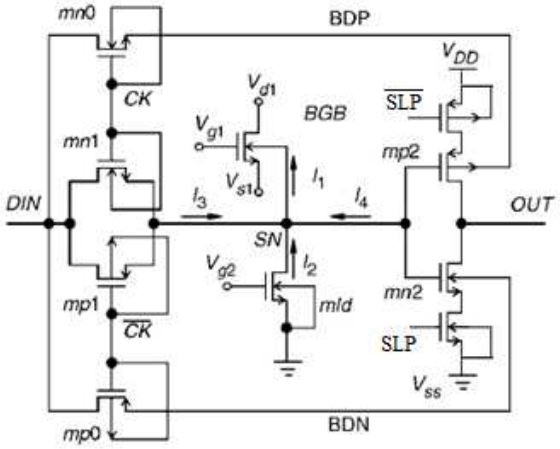


Fig. 2

$V_{d1} = 2.0\ V,\ V_{g1} = 0.5\ V,\ V_{s1} = 0.7\ V,\ V_{g2} = 0.53\ V$

In proposed work we used BGB-DTMOS technique along with the sleep transistors in the output inverter in order to reduce the leakage power dissipation in the standby mode. This technique is very effective and easy to implement in CMOS based circuits as the reduction in the leakage power is obtained by the addition of only two transistors and hence area overhead is also less.

IV. SIMULATION

All simulations are done using 180nm technology. All n-channel devices have a width of 360nm, and all p-channel devices have a width of 540nm. V_{DD} is chosen to be 0.6 V to DTMOS and V_{DD} is chosen to be 1.8 V for CMOS latch and BGB latch. All simulations are performed by using tanner tool.

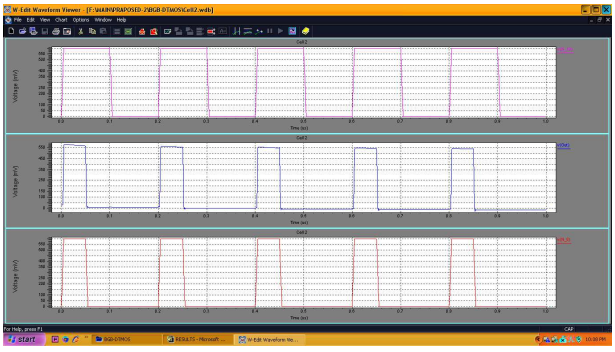


Fig 3. Simulated waveform of proposed technique.

V. RESULTS

A DTMOS-BGB DFF is formed by cascading a pair of master and slave latches shown in Fig. 1(c), and simulated by implementing it as a divide-by-two counter.

Table 1: Simulated results of different static DFFs for given technology.

DFF	VDD (V)	Power Delay Product (μW*ns)	P_{avg} (μW)	P_s (μW)	Delay (ns)
PROPOSED	0.6	1.097	1.066	0.00035	1.03
DTMOS-BGB	0.6	0.066	0.015	0.12	4.40
DTMOS	0.6	2.592	0.11	1.27	23.57
CMOS-BGB	1.8	0.495	0.64	0.22	0.773
CMOS	1.8	103.999	1.03	72.4	100.97

It is clear from the above table that the proposed technique provides better performance as it reduces the standby power consumption as compare to DTMOS-BGB latch, DTMOS latch, CMOS-BGB latch and CMOS latch. Also the proposed technique reduces the delay as compare to DTMOS-BGB latch, DTMOS latch, CMOS-BGB latch and CMOS latch. This technique can be easily implemented in CMOS based circuits. The drawbacks of this technique are that it adds two extra sleep transistors in the main circuit which increases area and average power consumption, but these drawbacks may be ignored as we are getting good performance in terms of standby power consumption and delay.

VI. CONCLUSION

In this paper low power DFF is Proposed and it reduces the standby power and delay as compare to other techniques, like DTMOS-BGB latch, DTMOS latch, CMOS-BGB latch and CMOS latch. A novel DFF utilising DTMOS, BGB devices and sleep transintors has been proposed and verified to be suitable for ultra-low voltage operation.

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