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Synchronization Problems in Synchronous Digital Hierarchy (SDH) Communication System and Master Slave Strategies

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Abstract:-

SDH is a well known technology which is used for the data communication. It is used for high speed data transmission. The synchronization in this technology is with respect to the single clock pulse. So different signals of different data rate are multiplexed by the same clock pulse. This paper is a review paper regarding the problems in synchronisation of the different data rate signals in single clock, and master slave technique used to overcome these problem.

1 .Introduction

SDH is a well known technology used in digital communication system. The plenty of overhead capacity and cross connect capability make SDH to be the well alternative for the pre existing PDH system. The compatibility between PDH is one of the major advantages of SDH technology . Traditionally, transmission systems have been asynchronous, with each terminal in the network running on its own recovered clock timing. In digital transmission, "timing" is one of the most fundamental operations.

Since these clocks are not synchronised, large variations can occur in the clock rate and thus the signal bit rate. For example, an E3 signal specified at 34 Mbit/s ±20 ppm (parts per million) can produce a timing difference of up to 1789 bit/s between one incoming E3 signal and another. Asynchronous multiplexing uses multiple stages. Signals such as asynchronous E1s (2 Mbit/s) are multiplexed (bit-interleaving), extra bits are added (bit-stuffing) to account for the timing variations of each individual stream and are combined with other bits (framing bits) to form an E2 (8 Mbit/s) stream. Bit-interleaving and bit-stuffing is used again to multiplex up to E3 (34 Mbit/s). The E1s are neither visible nor accessible within an E3 frame. E3s are multiplexed up to higher rates in the same manner. At the higher asynchronous rate, they cannot be accessed without de multiplexing. In a synchronous system, such as SDH, the average frequency of all clocks in the system is the same. Every slave clock can be traced back to a highly stable reference clock. Thus, the STM-1 rate remains at a nominal 155.52 Mbit/s, allowing many synchronous STM-1 signals to be multiplexed without any bit-stuffing. Thus, the STM-1s are easily accessed at a higher STM-N rate. Low-speed synchronous virtual container (VC) signals are also simple to interleave and transport at higher rates.

The synchronisation in SDH system is one of the challenge .because it is major issue for the telecom operators. Timing and synchronisation are the core technologies for SDH system.for the designinnig and implementation of SDH technology , synchronization is one of the intrinsic and essential factor. This paper will focus on some synchronization problems in SDH ,SDH equipment Clock(SEC),Strategies which can be used to synchronise the SDH a network. What is a timing loop and how to avoid the timing loop.

2. SDH Equipment Clock(SEC)

As discussed before SDH has lots of similarities with the PDH system and has a very good future in the field of high speed communication. But the timing in a SDH network is not as easy as in PDH system because the timing here which is mapped in a STM-N frame is cannot be trusted due to the addition of stuffed bits. So the SDH equipment which is incorporated in the function of clock pulse generation, filtration and the extraction of the signals is called as SDH Equipment Clock or SEC. The SEC is used to transfer the clock pulse to various STM-N frames which are multiplexed in the SDH system at different data rates as SDH supports variable data rate transmission. This is clock pulse can only be affected due to the delay in transmission line and not by bit stuffing or mapping of the frames. Digital switches and digital cross-connect systems are commonly employed in the digital network synchronisation hierarchy. The network is organized with a master-slave relationship with clocks of the higher level nodes feeding timing signals to clocks of the lower-level nodes. All nodes can be traced up to a Primary Reference Clock (PRC). So in any SDH system there all number of different clocks. Now if the link of all the master and slave clock pulses fails then also the synchronizing device should have the capability of maintaining operation with a well performance. So the function of SEC is to be used as a timing source in SDH system. The figure 1 shows the block diagram of SEC.

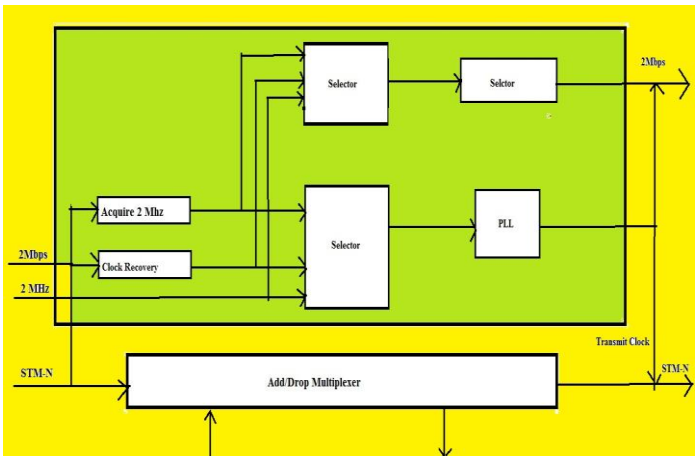

Figure 1 SEC

It has a 2MHz which is the basic clock pulse of STM –N signal, the selector blocks are used to select a particular channel. The operation of the filtration is done using a digital PLL . This helps in reduction in number of components and hence the cost of the system, Power consumption and Reliability of the system .The figure 2 shows the block diagram of digital PLL associated in SEC.

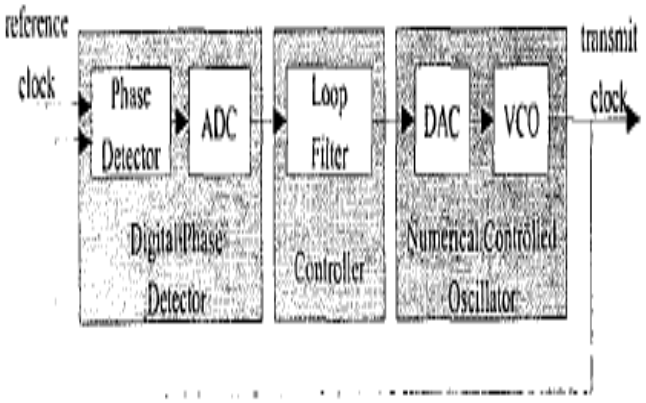

Figure 2 PLL in SEC

3. Master Slave Technology of Digital Synchronization Network

Synchronization in SDH system can be easily done by the help of master slave technology as it is more reliable as compared to mutual network synchronization. The main principle of master slave technology is to distribute the main clock pulse or say the master clock pulse in different types of other clocks known as the slave clock. This distribution may be done directly or indirectly depending on the conditions. The figure 3 is showing the Master Slave Technology distribution of clock distribution.

In the figure it is shown that the master clock pulse is shared or distributed among the various network equipments called as slaves so

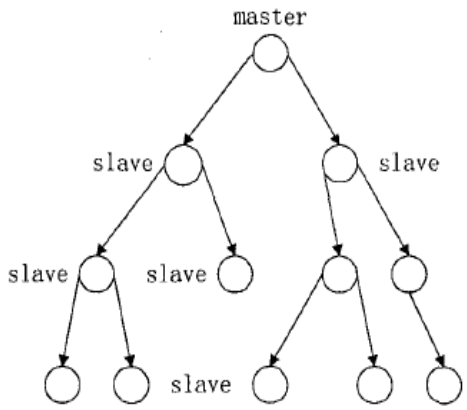

Figure 3 Master Slave strategies

The clock is a shared resource that can be served to various equipments. So the reliability of the master clock is very important issue in case of network synchronization in master slave technology.

4. Issues related to Master Slave Strategy:-

As discussed above the master slave technology is totally based on the master clock pulse. So there should be a backup in case of failure of the reference clock pulse. Once the master clock is failed the whole network will become a synchronized and hence will cause undesirable effects. So it is necessary to have a reliable master clock in the SDH synchronization system. Similarly the SEC also plays an important role in master slave technology as it is use to recover. Trace and distribute the clock pulse. SEC is connected to all the slaves using different paths. So there should be two different paths as when one distribution path fails the clock can be synchronized using the alternative path. The last consideration which should be taken in account is the length of the distribution path. For the Master Slave technology, the length of the path should be as short as possible. When the timing is distributed through the STM-N, its quality will degrade as it passes through the number of networks of the slave clocks. The error in the reference clock pulse will also increase due to noise in the distribution chain and the changes in temperature. According to ITU T recommendations there can be 20 network elements in one chain without a slave element and can have up to 10 slave elements.

5. Conclusions:-

Synchronisation is indeed an issue in SDH frame implementation as it is Byte synchronized and not bit synchronized. Although master slave technique and SEC technique is used, for low data rate signals, bit stuffing is used. In my work I have studied about the master slave technique and SEC. However future work will be based on the reduction of stuffed bits so that data rate can be increased in future.

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