International Journal of Scientific Engineering and Technology (ISSN : 2277-1581)
www.ijset.com, Volume No.1, Issue No.2 pg:59-64 01 April 2012

Superiority of Current mode over Voltage mode Interconnects

Yash Agrawal,Rohit Dhiman, Rajeevan Chandel

Department of Electronics & Communication Engineering
National Institute of Technology, Hamirpur 177 005, Himachal Pradesh, India
mr.yashagrawal@gmail.com, rohitdhiman.nitham@gmail.com, rajevanchandel@gmail.com

***Abstract*- In deep submicron VLSI circuits, interconnect delays dominate MOSFET gate delays. Conventional buffer insertion method reduces delays at the cost of valuable chip area. Consequently, alternative methods are essential. Current mode interconnects have lesser delay than voltage mode circuits and also consume lesser chip area. In the present work, superiority of current mode over voltage mode interconnects is analyzed. The simulative analysis is carried out using Tanner EDA tools.**

I. INTRODUCTION

Interconnects are supposed to be skeleton of VLSI circuits but today it is acting as a major bottleneck. With technology scaling, device dimensions are decreasing. This is reducing device delay. However advancements in VLSI technology lead to increase in chip size. Scaled technologies and larger chip size facilitates huge chip functionality. This increases interconnect lengths, which in turn increases signal propagation delays. Thus at DSM technologies, the interconnect delays are becoming dominant than gate delays. Also, signal at the output are getting more distorted and noisy. Cross-talk effects are getting introduced due to increasing resistive and capacitive parasitics (R and C) of the interconnects. Interconnect design is thereby becoming major challenge for the VLSI design engineers. Hence alternative design methods are required to optimize and have better performance of the systems.

Buffer insertion is an important method proposed by researchers to reduce long interconnects delays [1-4]. In buffer insertion, buffers are introduced in between the interconnects modeled as RC load. This reduces overall delay but at the same time, it requires high chip area and also increases power dissipation in the circuit [5-7].

Current mode interconnects are reported by various researchers to reduce interconnect delays [8-11]. In current mode interconnects, information is conveyed using current signal rather than voltage signal. It has very low output impedance. The current mode interconnects have higher performance as compared to voltage mode circuits. The current mode interconnects have less delay, less effect of supply voltage reduction and voltage swing reduction. It has higher bandwidth and less vulnerable to electrostatics discharge (ESD) [12]. The voltage and current mode interconnects are analyzed using SPICE simulations in the present work.

The paper is arranged as follows. Section I introduces the topic. Section II deals with voltage mode interconnects. Section III describes the current mode interconnects. In section IV, superiority of the current mode interconnects over voltage mode interconnects is established. Section V presents results and discussions. Finally, conclusions are drawn in section VI.

II. VOLTAGE MODE INTERCONNECTS

Voltage mode signaling is most widely used in VLSI chips. In voltage mode signaling, receiver provides high input impedance (ideally infinity). The information is conveyed in the form of voltage. The output voltage is a function of input signal and is varied according to supply voltage. Fig.1 shows the theoretical model of conventional voltage mode interconnect implementation [10]. The output is terminated by an open circuit.

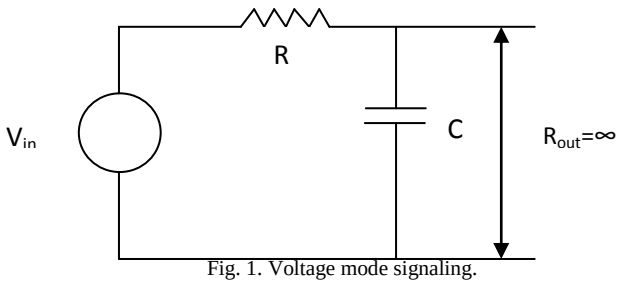

Fig. 1. Voltage mode signaling.

CMOS representation of voltage mode is shown in Fig. 2 [1,3]. The driver consists of an inverter which drives long RC interconnect chain. This is terminated by high input impedance of the inverter circuit at the receiver. This high input impedance of the receiver gives rise to high input capacitance which leads to high charging and discharging time for RC interconnect chain. Hence voltage mode signaling has large delay. Due to high input impedance at the receiver, the charge accumulated at the input of the receiver does not get effective

discharge path to ground as a result this may cause electrostatic induced gate oxide break down.

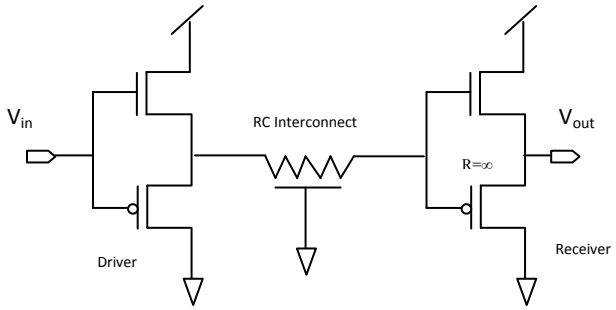

Fig. 2. CMOS representation of voltage mode signaling [10].

III. CURRENT MODE INTERCONNECTS

In current mode signaling, information is represented as current signal. The receiver provides low impedance (ideally zero) at its input. In current mode signaling line is terminated by shorting the wire. The theoretical model of current mode signaling is as shown in Fig. 3 [10].

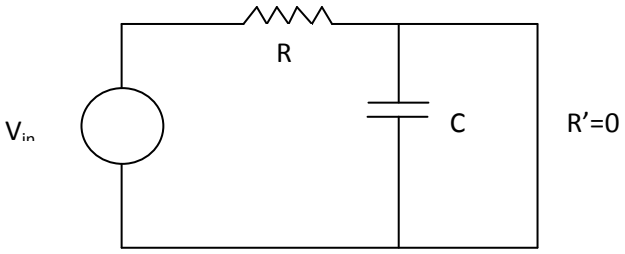

Fig. 3. Current mode signaling.

The CMOS representation of current mode signaling is shown in Fig. 4. The receiver senses current signal at its input and provides low impedance.

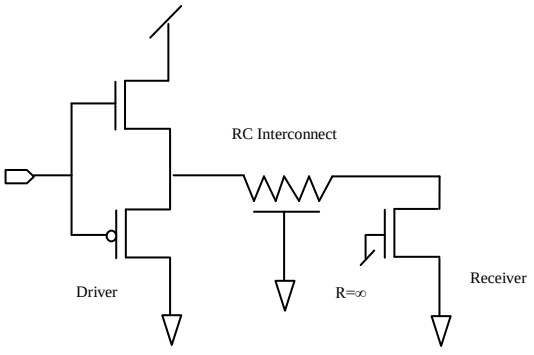

Fig. 4. CMOS representation of current mode signaling [10].

Current mode interconnects have various advantages over voltage mode. These are discussed in section IV.

IV. COMPARATIVELY ANALYSIS OF CURRENT MODE AND VOLTAGE MODE INTERCONNECTS

Depending on the signal carriers of data links, wire channels can be classified as voltage mode or current mode signaling. The interconnects using current mode signaling scheme gives better results and performance as compared to interconnects using voltage mode signaling. The various advantages of current mode interconnect over voltage mode interconnects are discussed as follows.

A. Delay

As technology is shrinking, interconnect delays are increasing and is dominating transistor gate delay. This reduces speed of the circuit and may give undesired results at the output. Interconnects using voltage mode signaling scheme such as buffer insertion is found to be effective in reducing delay but it requires extra chip area and also power dissipation due to buffer increases. In current mode interconnects low impedance is provided at the output. It is found that current mode interconnect circuits gives lesser delay as compared to voltage mode.

Mathematically, average rising or falling delay in the circuit can be given as [13]:

$$Delay = \frac{C\Delta v}{\Delta I_{avg}} \quad (1)$$

where, C is the capacitance of the node. Δv is the voltage swing of the node and I_{avg} is the average charging/ discharging current. From (1), it can be seen that either by reducing voltage swing or by increasing charging and discharging current, delay can be reduced. In voltage mode circuits, voltage swing cannot be reduced since it is limited by signal to noise ratio requirements. However charging and discharging current in current mode circuits can be increased [13]. This will give lesser delay and hence current mode circuits can give faster transient response.

B. Voltage swing reduction

Current mode circuits can be operated for lower voltage swings of input signals as compared to voltage mode circuits. The output of voltage mode circuits is directly proportional to input signal variations. It gives noisy or distorted output at reduced input voltages swings. The input voltage swing is limited by signal to noise ratio and cannot be reduced below certain limit. It results in slower response of the circuit.

C. Supply voltage reduction

The effect of supply voltage and ground fluctuations has adverse effects in voltage mode circuits. This is because output varies directly with input signal in voltage mode circuits while in current mode signaling output is in current form and there is very less attenuation due to supply voltage reduction.

D. Bandwidth Improvement

The current mode interconnect provides higher bandwidth as compared to voltage mode circuits. Due to higher bandwidth in current mode circuits, signals can be transmitted fast over the link and hence it will increase the speed of operation.

E. Electrostatic discharge (ESD)

As devices are shrinking, the thickness of gate oxide is also scaling down. As a result, there is increase in ESD induced MOSFET failures due to breakdown of gate oxide insulators. Voltage mode circuits are more vulnerable to this as it has high input impedance [13]. The electrostatic charges accumulates at the input of gate as of because high input impedance of voltage mode circuits. However, low input impedance in current mode circuits prevents accumulation of electrostatic charges at the input terminal of the gate and is therefore a more safe design technique.

V. RESULTS AND DISCUSSION

Firstly, the current and voltage mode interconnects are analyzed. The schematic of voltage and current mode circuit is shown in Fig. 5 and 6.

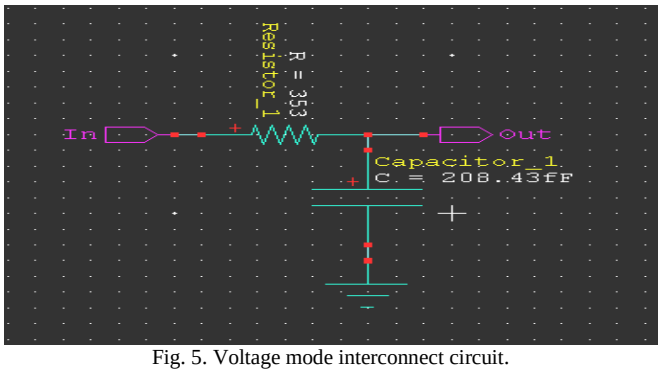

Fig. 5. Voltage mode interconnect circuit.

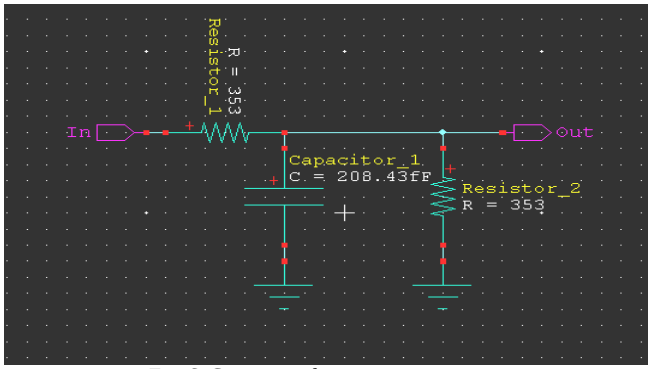

Fig. 6. Current mode interconnect circuit.

Output waveforms of voltage and current mode circuit are as shown in Fig. 7 and 8.

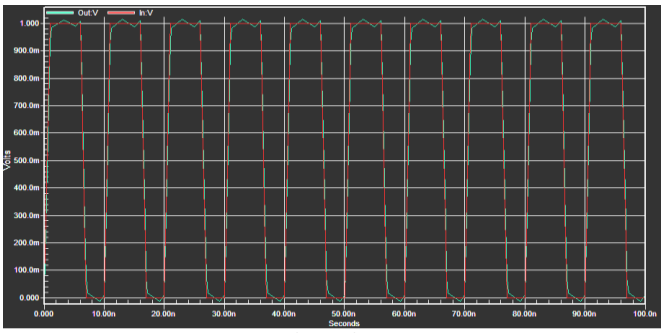

Fig. 7. Output waveform of voltage mode circuit.

It can be seen from Fig. 7 that output and input waveform coincides with each other.

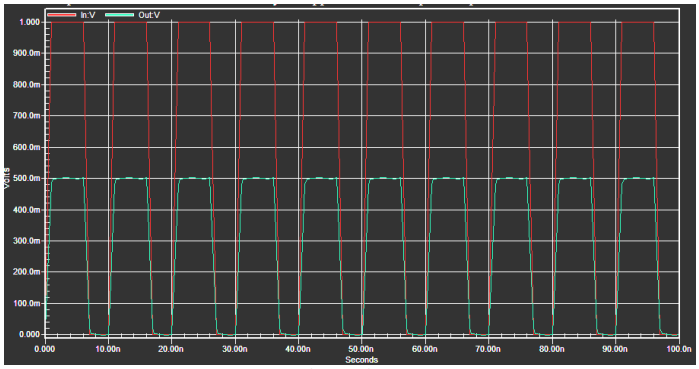

Fig. 8. Output waveform of current mode circuit.

From Fig. 8, it can be seen that output voltage is reduced. In current mode circuits information is conveyed in the form of current. Therefore the voltage signal is reduced to a much lower value.

The delay analysis is carried out using NAND gate at driver. The schematic for current mode interconnects is as shown in Fig. 9.

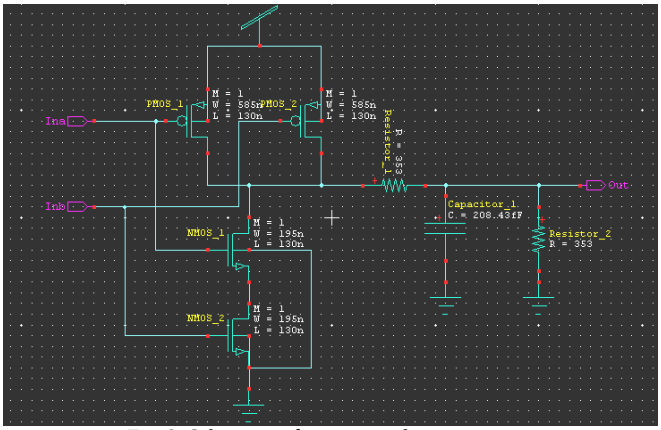

Fig. 9. Schematic of current mode interconnect.

Table I
Delay Analysis for voltage and Current Mode Interconnects [13, 14].

Signaling mode	Delay (ns)	P (VDD) (µw)	P(Vina) (nw)	P(Vinb) (nw)	P (Total) (µw)	PDP (10^{-15})
Voltage mode	2.58	21.89	66.77	42.94	22.01	56.78
Current mode	0.520	115.03	28.88	21.48	115.08	59.84

Table I shows the delay analysis for both voltage and current mode interconnects [13-14]. It is analyzed that with current mode interconnects delay decreases from 2.58ns to 0.52ns however power dissipation in the circuit increases from 22.01µw to 115.08µw. This is due to the low impedance at the receiver of current mode interconnect circuit. The overall figure of merit power-delay-product (PDP) of current mode increases from $56.78x10^{-15}$ to $59.84x10^{-15}$. This shows the better performance and superiority of current mode over voltage mode interconnects.
The delay analysis for current and voltage mode interconnect is shown in Fig. 10. It is seen that there is 79.84% reduction in current mode interconnect delay.

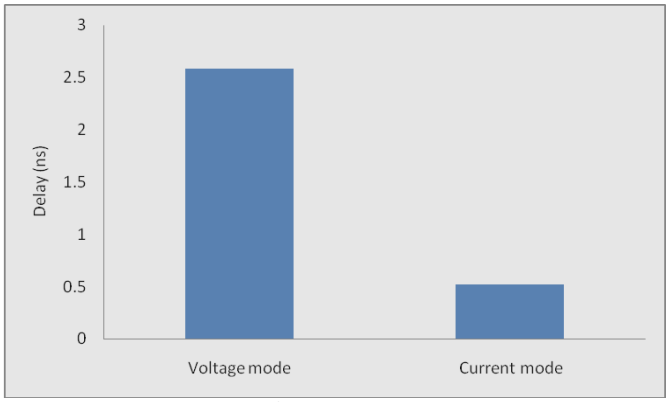

Fig. 10. Delay analysis of current and voltage mode interconnects.

The effect of voltage swing reduction is also analyzed. For this supply voltage is kept at 1V and NAND gate input values (Fig. 9) are varied.
For first case it is kept at 1V and in second case 0.5V.
The current mode is compared with voltage mode buffer circuit. The waveforms are as shown in Fig. 11 and 12.

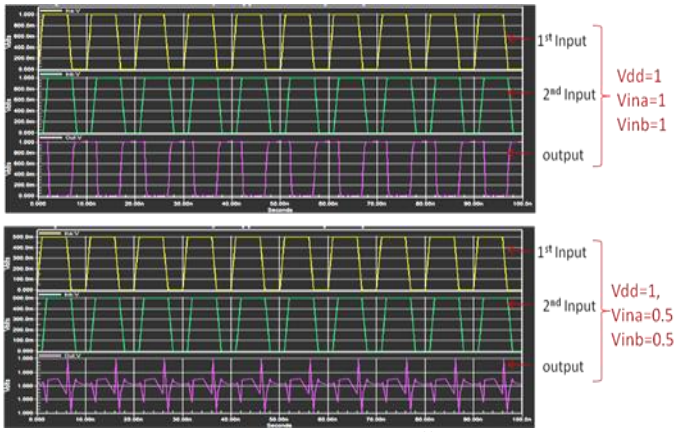

Fig. 11. Input voltage swing reduction in buffer inserted voltage mode interconnect.

It can be seen from Fig. 11 that output waveform at a reduced voltage swing is getting much distorted.
Fig. 12 shows the output waveform for current mode circuits, for the same two cases.

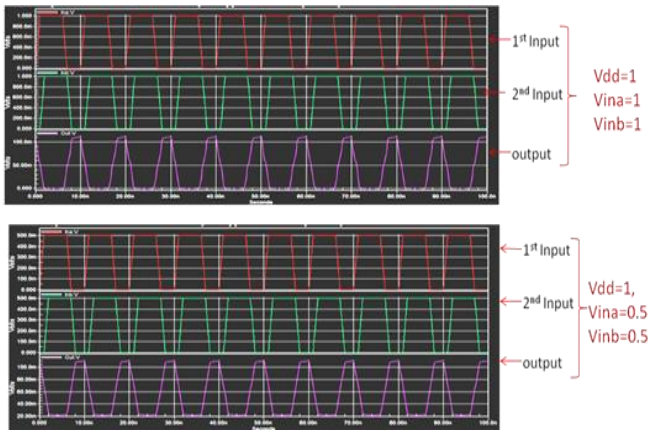

Fig. 12. Input voltage swing reduction in current mode interconnect.

The investigations show that the output waveform of current mode circuit is very less affected at reduced voltage as compared to voltage mode buffer inserted circuit. This shows that current mode interconnect circuits can work satisfactory at lower voltage swings.

Further, the effect of supply voltage (Vdd) reduction for voltage mode buffer inserted and current mode interconnect circuit is analyzed. The input signals of NAND gate is kept

constant at 1V and supply voltage is varied from 1V to 0.3V. The waveforms are as shown in Fig. 13 and 14.

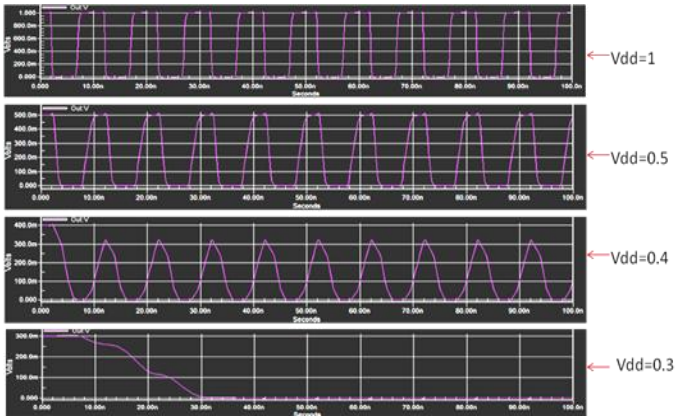

Fig. 13. Effect of supply voltage reduction in buffer inserted voltage mode interconnect.

Fig. 13 shows output signals for buffer inserted voltage mode interconect at different supply voltages. It can be seen that output signal gets totally distorted at a scaled voltage Vdd=0.3V.

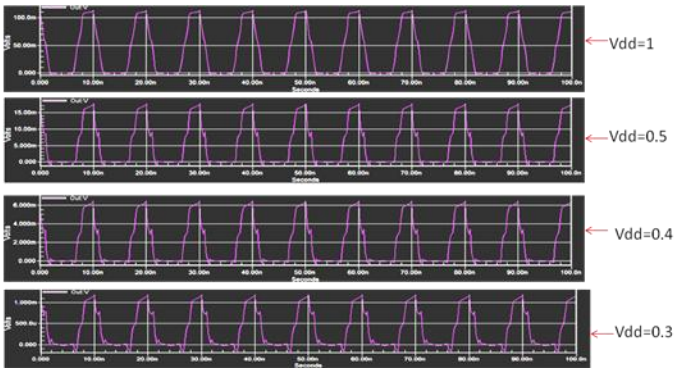

Fig. 14. Effect of supply voltage reduction in current mode interconnect.

Fig. 14 shows the output signals for current mode interconnect circuit at different supply voltages. It can be seen that the output signals remain almost same even at highly scaled supply voltage of 0.3V.

Thus it is inferred that current mode circuits can work at much lower supply voltages. Also, with technology scaling, supply voltage gets reduced. Hence current mode circuits could be more beneficial at lower technologies.

Current mode interconnect circuits have higher bandwidth as compared to voltage mode interconnect circuits. For this, frequency or ac analysis is carried out. Fig. 15 shows the frequency spectrum for voltage mode and current mode interconnect circuits.

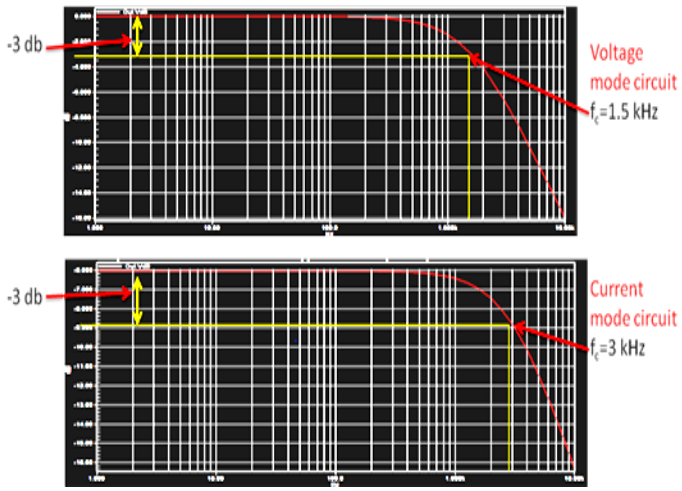

Fig. 15. AC analysis for voltage and current mode interconnects.

The voltage mode circuit shows a cut-off frequency of 1.5 KHz while that of the current mode circuit is 3 KHz. Hence the latter has higher (double) bandwidth than the former. This establishes that the current mode interconnects have higher speed compared to voltage mode ones.

VI. CONCLUSIONS

Current mode and voltage mode interconnects are analyzed in the present work. It is analyzed that the current mode signaling has large benefits over the voltage mode signaling. In deep submicron technologies interconnect delay dominates gate delay. Interconnects using current mode signaling can have lesser delay along with various other benefits. The current mode interconnect circuits are less affected by supply voltage fluctuations and reduced voltage swings. These have higher bandwidth over voltage mode circuits and also are less vulnerable to ESD induced MOSFET failures. All these advantages give current mode signaling an upper edge over the voltage mode signaling. At highly miniaturized technologies, interconnects with current mode signaling would be the best choice.

ACKNOWLEDGEMENT

The authors acknowledge with gratitude the technical and financial support from Ministry of Communications & Information Technology, DIT, Govt. of India, New Delhi, through VLSI SMDP-II and NPMASS Projects at NIT Hamirpur (HP), India.

REFERENCES

[1] V. Adler, and E.G Friedman, "Repeater design to reduce delay and power in resistive interconnect," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, pp. 607-616, 1998.

[2] V. V.Deodhar, and J. A. Davis, "Voltage scaling, wire sizing and repeater insertion design rules for wave-pipelined VLSI global interconnect circuits," *Sixth International Symposium on Quality of Electronic Design*, pp. 592-597, 2005.

[3] R. Chandel, S. Sarkar, and R.P. Agarwal, "An Analysis of Interconnect Delay Minimization by Low-Voltage Repeater Insertion," *Microelectronics Journal*, *Elsevier Science*, vol. 38, no. 4-5, pp. 649-655, April-May 2007.

[4] R. Dhiman, and R. Chandel, "Sub Threshold Delay and Power Analysis of Complementary Metal-Oxide Semiconductor Buffer Inserted Interconnect for ultra Low Power Applications," *Journal of Low Power Electronics, ASP*, vol. 8, no.1, 2012.

[5] Nalamalpu and W. Burleson, "A practical approach to DSM repeater insertion: satisfying delay constraints while minimizing area and power," *14th Annual .IEEE Int. ASIC/SOC Conf.*, pp. 152-156, 2001.

[6] H. Shah et al., "Repeater insertion and wire sizing optimization for throughput centric VLSI global interconnects," *Proc. IEEE Int. Conf. on Computer Aided Design (ICCAD)*, pp. 280-284, 2002.

[7] J. Eble, V. De, D. Wills, and J. Meindl, "Minimum repeater count, size and energy dissipation for giga scale integration interconnects," *Proc. IEEE Int. Interconnect Technology Conf. (IITC)*, pp. 56-58, 1998.

[8] R. Bashirullah, Wentai Liu, and R. K. Cavin, "Current-mode signaling in deep sub micrometer global interconnects," *IEEE Transactions on VLSI Systems*, vol. 11, pp. 406-417, 2003.

[9] A. Katoch, H. Veendrick, and E. Seevinck, "High Speed Current Mode Signaling Circuits for On-chip Interconnects," IEEE International Symposium on Circuits and Systems, vol. 4, pp. 4138-4141, 2005.

[10] A. Maheshwari, and W. Burleson, "Current sensing Technique for Global Interconnects in Very Deep Submicron (VDSM) CMOS," IEEE Computer Society Workshop on VLSI, pp. 66-70, 2001.

[11] R. Bashirullah, Wentai Liu, and R. Cavin, "Delay and power model for current-mode signaling in deep submicron global interconnects," *Proceedings of the IEEE Conference*, pp. 513-516, 2002.

[12] R. Kar, K. R. Reddy, A. K. Mal, and A. K. Bhattacharjee, "An explicit approach for bandwidth evaluation of on-chip VLSI RC interconnects with current mode signaling technique," *International Conference on Computing Communication and Networking Technologies* (ICCCNT), pp. 1-4, 2010.

[13] Fei Yuan, CMOS Current-Mode Circuits for Data Communications, Springer

[14] International Technology Roadmap for Semiconductors (ITRS), 2009 update. [Online document], Available http://public.itrs.net.