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Design of Current Mode Interconnect Receiver Subsystem for High Performance Applications

Yash Agrawal[#1], Rohit Dhiman[#2], Rajeevan Chandel[#3]

Department of Electronics & Communication Engineering
National Institute of Technology, Hamirpur-177 005 HP India
[1]mr.yashagrawal@gmail.com, [2]rohitdhiman.nitham@gmail.com, [3]rajevanchandel@gmail.com

Abstract- A receiver subsystem for current mode interconnects is presented in the present paper. It is shown that current mode interconnects shows better performance compared to voltage mode interconnect circuits. The current mode interconnect system using proposed receiver subsystem shows about 15% lesser latency and 40% increased throughput. Effect of voltage scaling on power dissipation for current mode (CM) and voltage mode (VM) has been analyzed. Current mode interconnects shows lesser power dissipation compared to voltage mode circuits. Analysis has been carried out using SPICE in 0.18 µm technology.

I. INTRODUCTION

Interconnects are one of the essential parts of the VLSI chips. As technology scales down, device dimensions decreases but at the same time chip dimensions increases in order to embed more and more devices on the same chip. As a result, global interconnects causes major delays in the circuits. At deep sub micron (DSM) technologies these delays are even more than gate delays and hence need to be reduced [1]. Various techniques to improve the performance of interconnects has been proposed [2].

Repeater insertion method has been suggested by many researchers [3, 4]. But there is some practical limitations to the performance improvement [5]. Moreover repeaters need to be proper sized and should be fixed at proper intervals to achieve optimum results. As an alternative approach to improve the performance of interconnects, current mode signaling has been proposed [6-7, 13].

In the present paper, current mode signaling for interconnect system has been analyzed. Receiver design using transmission gates for current mode interconnect system has been carried out. It is shown that the current mode system using proposed receiver has lesser delay and higher throughput than voltage mode interconnect circuits.

The rest of the paper is organized as: section II gives a brief overview of current mode interconnect system. In section III current mode receiver is described. Section IV gives simulation methodology. Results and discussions are made in section V. Section VI gives conclusion.

II. CURRENT MODE INTERCONNECT SYSTEM

In current mode, information is represented in current signals. Current mode interconnect system consists of a driver, receiver and a decoder subsystems [8, 9]. The function of the driver is to convert input voltage signals into analog multilevel current signals. As current signals are represented as multilevel, hence multiple input voltage signals can be send as a single multilevel current signal over the interconnect line. This is beneficial in reducing delay across the interconnect lines. Also, it is desired to have high driver output impedance. This reduces noise injection in the circuit. The receiver subsystem converts this analog multilevel current signal into thermometer code signals [10]. The thermometer codes changes only one bit each time and hence is beneficial in reducing glitches at the output. Also thermometer codes are necessary in order to distinguish '10' and '01' input current levels. These thermometer codes are then given to decoder circuit. The decoder circuit converts back these thermometer codes into original voltage signal. The block diagram representation of complete current mode interconnect system is shown in fig. 1.

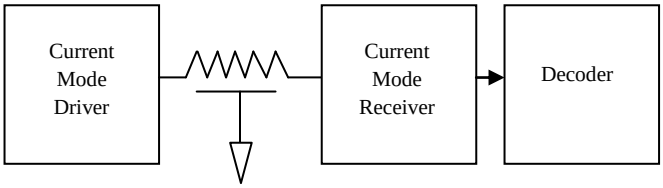

Fig.1 Block Diagram of Current Mode Interconnect System

III. THE RECEIVER SUBSYSTEM

The receiver subsystem is shown in figure 2. It consists of a current to voltage converter, three comparator circuits and inverter circuits for full output voltage realization. Transmission gates are realized using CMOS technology.

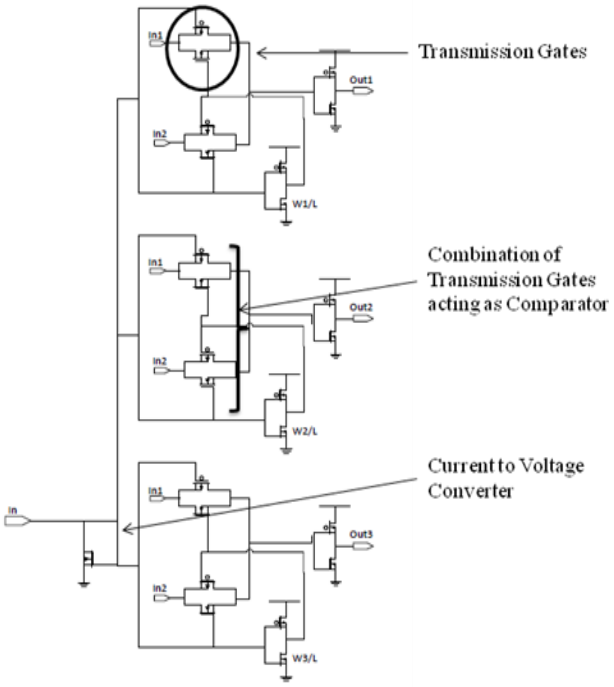

Fig.2 The Receiver Subsystem

The operation of the receiver subsystem can be seen as: the multilevel current signal coming from driver and interconnect subsystem is given to current to voltage converter. This is then given to the comparator circuit. The combination of transmission gates forms a mixer circuit which basically acts as a comparator circuit. The threshold values of the three comparators are varied by varying the width to length ratio of the inverters used in the comparator circuit. These threshold values are varied in order to have different pinch-off values for different comparator circuits.

The inverter circuit used in the comparator circuits operates in between linear and saturation region. The current in saturation and linear region through MOSFET can be given in eqs (1) and (2) respectively as [11, 12].

$$I_d = \mu_{eff} C_{ox} (W/L)(V_{gs} - V_{th})^2 \quad (1)$$

$$I_d = \mu_{eff} C_{ox} (W/L)\left[(V_{gs} - V_{th})V_{ds} - 2V_{ds}^{\ 2}\right] \quad (2)$$

where, I_d is drain current, μ_{eff} is the effective mobility, C_{ox} is the gate oxide capacitance, W is channel width, L is the length of gate, V_{th} is the threshold voltage, V_{gs} and V_{ds} are gate and drain voltage respectively.

The different comparators have different threshold voltage. Depending on this, width to length ratio for different comparator circuits can be calculated using eqs. (1) and (2). Also, condition for saturation and linear state for N-MOSFET is given in eqs. (3) and (4). As $(V_{gs} - V_{th})$ becomes greater than V_{ds}, the inverter output used in the comparator circuit switches from logic high to logic low value. Due to variation in dimensions of inverter circuit of all the comparators, they switch at different values of V_{gs} for different comparator circuits.

$$V_{ds} > (V_{gs} - V_{th}) \quad (3)$$

$$V_{ds} < (V_{gs} - V_{th}) \quad (4)$$

The output waveform of the receiver subsystem is shown in section V.

IV. SIMULATION METHODOLOGY

The simulation is carried out using SPICE at 0.18 um technology. The interconnect is modeled as four section π network. The resistance (R) and capacitance (C) value are calculated mathematically [14]. The value of R and C so calculated are 0.070 MΩ/m and 270 pf/m respectively. The value of power supply voltage is taken as 1.8 V.

The complete circuit diagram of current mode interconnect system is shown in figure 3. It comprises of a driver, interconnect system, receiver subsystem and a decoder. The input-output waveforms of the current mode interconnect system is given in section V.

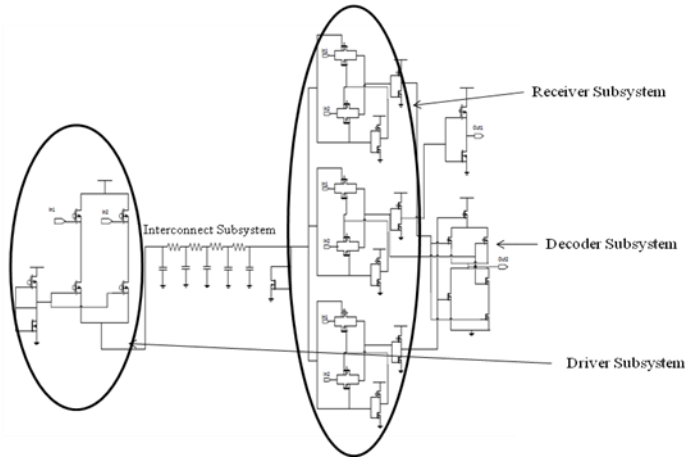

Fig. 3 Circuit Diagram of Current Mode Interconnect System

V. RESULTS AND DISCUSSIONS

Figure 4 shows the input and output signals of proposed current mode receiver subsystem. The output consists of thermometer codes which are then given to decoder circuit to regain the original voltage signal.

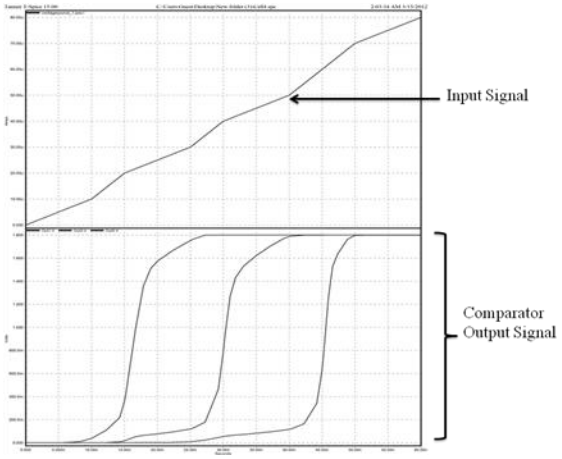

Fig.4 Output waveforms of Receiver Subsystem

Figure 5 shows the input-output waveforms of the complete current mode system using proposed receiver.

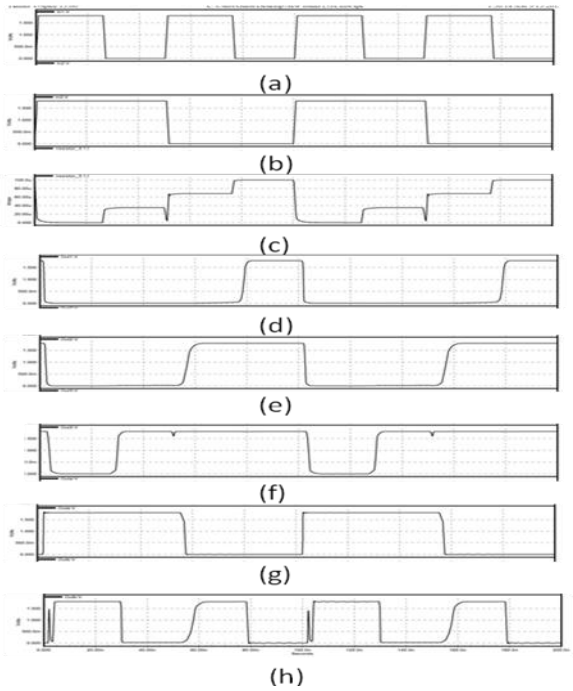

Fig. 5 Waveforms of the Complete Current Mode Interconnect System

The input voltage signal to the driver is shown in 5(a) and (b). 5(c) shows the analog current output waveform of the driver subsystem. This is converted into thermometer codes using receiver subsystem as shown in 5(d), (e), (f). The original voltage signal is regained at the output of decoder and is shown in 5(g) and (h).

Figure 6 shows the delay versus interconnect length plot. For global interconnects the current mode system with proposed receiver system shows less delay.

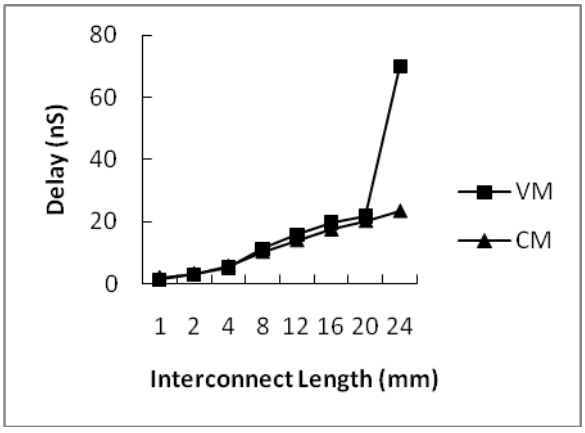

Fig. 6 Delay vs. Interconnect system

Figure 7 gives the throughput as a function of interconnect length. It shows higher throughput. For example at interconnect length of 1 mm, current mode interconnect shows 50% higher throughput than voltage mode interconnect system. Hence current mode circuits can be operated at higher data rates for transmission over interconnect line as compared to voltage mode circuits.

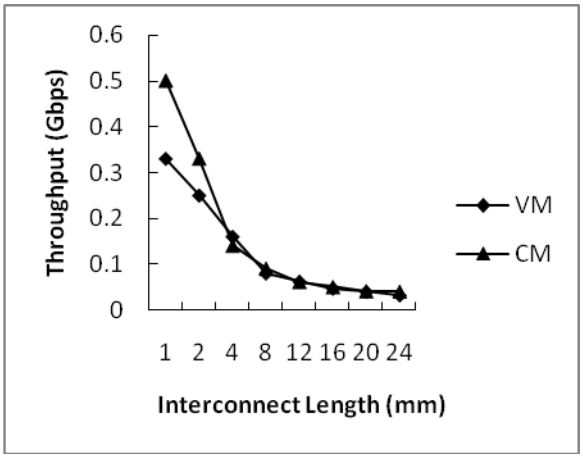

Fig. 7 Throughput vs. Interconnect system

Figure 8 shows the variation of average power versus V_{DD}. As can be seen that there is considerable reduction in power dissipation in current mode as compared to voltage mode interconnect system. For example, at V_{DD} value of 1.5V, power dissipation for current mode is 0.206 mW and for voltage mode is 0.32 mW.

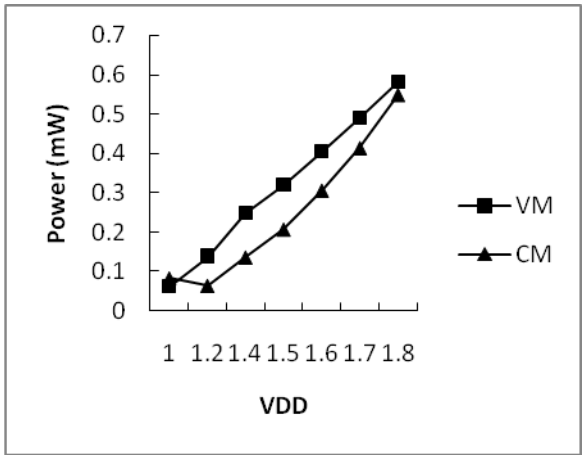

Fig. 8 Power vs. VDD

Figure 9 shows the plot of delay versus V_{DD}. Delay in current mode is lesser than voltage mode interconnect system. This is because of the fact that there is less charging and discharging of interconnect capacitances in current mode system.

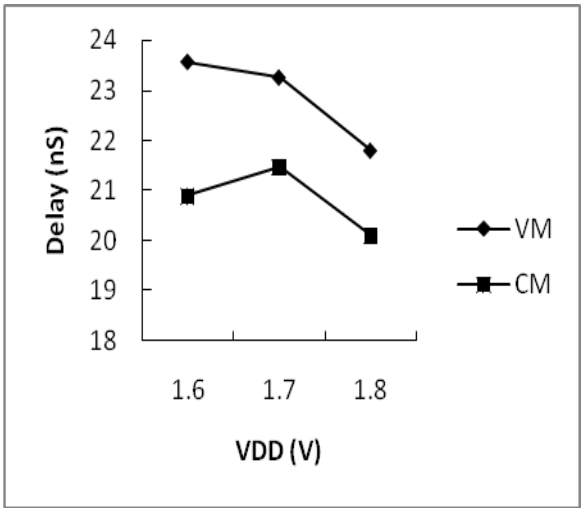

Fig. 9 Delay vs. VDD

Figure 10 shows the variation of power dissipation with temperature. The power dissipation in current mode interconnect system is lesser as compared to voltage mode interconnect systems. Hence current mode circuits could be operated at higher temperatures with minimum power dissipation in the circuit.

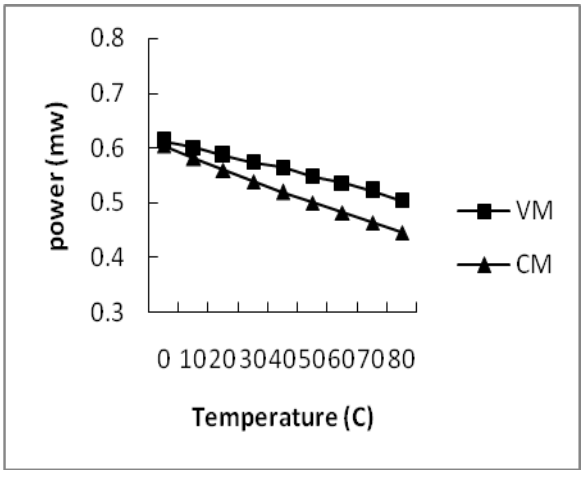

Fig. 11 power vs. Temperature

VI. CONCLUSION

The current mode interconnect system had been shown. It is shown that current mode interconnect system with the proposed current mode has lesser delay, power dissipation and higher throughput compared to voltage mode interconnect circuits. Hence current mode interconnect systems are better alternative than voltage mode interconnect systems for high performance applications.

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