International Journal of Scientific Engineering and Technology (ISSN : 2277-1581)
www.ijset.com, Volume No.1, Issue No.4, pg : 71-75 01 Oct. 2012

LLP in Chain Inverter by using CMOS Circuit

Ajay Sharma, C.D Khare, Anurag Garg, Sanjay verma
EC, EX Department, R.G.P.V. Bhopal University
S.V.I.T, Indore, I.P.S. Gwalior, India
sharma24@gmail.com

Abstract – This paper provide new low power solutions for Very Large Scale Integration (VLSI) designers. Especially, we focus on leakage power reduction. Although leakage power was negligible at 0.18µ technology and in nano scale technology, such as 0.07µ, leakage power is almost equal to dynamic power consumption. This paper presents heretofore unexplored methods for low-power VLSI design. In particular, the Low Leakage approach provides what may be the best solution for VLSI designers concerned about the twin problems of low static power and maintenance of VLSI logic state during sleep mode. For such a two-headed problem, the Low Leakage approach can provide two orders of magnitude (100X) or more static power reduction over the best prior approach; however, there is a cost potentially quite small – in terms of delay increase and area overhead. In short, Low Leakage principles provide heretofore unknown Pareto points for consideration in VLSI design.

Keywords: CMOS, Low Leakage, Static Power Dissipation

I. INTRODUCTION

Power consumption is one of the top concerns of Very Large Scale Integration (VLSI) circuit design, for which Complementary Metal Oxide Semiconductor (CMOS) is the primary technology. Today's focus on low power is not only because of the recent growing demands of mobile applications.

Even before the mobile era, power consumption has been a fundamental problem. To solve the power dissipation problem, many researchers have proposed different ideas from the device level to the architectural level and above. However, there is no universal way to avoid tradeoffs between power, delay and area, and thus designers are required to choose appropriate techniques that satisfy application and product needs.

Power consumption of CMOS consists of dynamic and static components. Dynamic power is consumed when transistors are switching, and static power is consumed regardless of transistor switching. Dynamic power consumption was previously (at 0.18µ technology and above) the single largest concern for low-power chip designers since dynamic power accounted for 90% or more of the total chip power. Therefore, many previously proposed techniques, such as voltage and frequency scaling, focused on dynamic power reduction.

However, as the feature size shrinks, e.g., to 0.09µ and 0.065µ, static power has become a great challenge for current and future technologies. Based on the International Technology

Roadmap for Semiconductors (ITRS) [1], Kim et al. report that sub threshold leakage power dissipation of a chip may exceed dynamic power dissipation at the 65nm feature size [2].

One of the main reasons causing the leakage power increase is increase of sub-threshold leakage power. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub-threshold leakage power increases exponentially as threshold voltage decreases. Furthermore, the structure of the short channel device lowers the threshold voltage even lower. In addition to sub-threshold leakage, another contributor to leakage power is gate-oxide leakage

Power due to the tunneling current through the gate-oxide insulator. Since gate oxide thickness will be reduced as the technology decreases, in nano scale technology, gate-oxide leakage power may be comparable to sub-threshold leakage power if not handled properly. However, we assume other techniques will address gate-oxide leakage; for example, high-k

dielectric gate insulators may provide a solution to reduce gate-leakage [2].

Therefore, this work focuses on reducing sub-threshold leakage power consumption.

In this work, we provide novel circuit structure named "Low Leakage" as a new remedy for designers in terms of static power. The Low Leakage has a novel structure that combines the advantages of two major prior approaches, the sleep transistor technique and the forced stack technique. However, unlike the sleep transistor technique, the Low Leakage technique retains the original state; furthermore, unlike the forced stack technique, the Low Leakage Technique can utilize high-Vth to achieve more than two orders of magnitude leakage power reduction compared to the forced stack.

Unfortunately, the Low Leakage technique comes with delay and area overheads. Therefore, the Low Leakage technique provides new Pare to points to designers who require ultra-low leakage power consumption and are willing to pay some area and delay cost. In

This work, we explore the basic structure of the Low Leakage. Also, we study various Low Leakage circuits including generic logic circuits and memory. We discuss the advantages and disadvantages of the Low Leakage and a technique to reduce the delay overhead.

II. PROBLEM STATEMENT

This work addresses new low power approaches for Very Large Scale Integration (VLSI) logic. Power dissipation is one of the major concerns when designing a VLSI system. Until recently, dynamic power was the only concern. However, as the technology feature size shrinks, static power, which was negligible before, becomes an issue as important as dynamic power. Since static power increases dramatically (indeed, even exponentially) in nano scale silicon VLSI technology, the importance of reducing leakage power consumption cannot be overstressed. A well known previous technique called the sleep transistor technique cuts off Vdd and/or Gnd connections of transistors to save leakage power consumption. However, when transistors are allowed to float, a system may have to wait a long time to reliably restore lost state and thus may experience seriously degraded performance. Therefore, retaining state is crucial for a system that requires fast response even while in an inactive state. Our research provides new VLSI techniques that achieve ultra-low leakage power consumption while maintaining logic state, and thus can be used for a system with long inactive times but a fast response time requirement.

III. LOW LEAKAGE APPROACH

In this section, we explain our low leakage structure comparing to the forced stack technique and the sleep transistor technique. The details of the low leakage inverter are described as an example. Two operation modes, active mode and sleep mode, of the low leakage technique are explored.

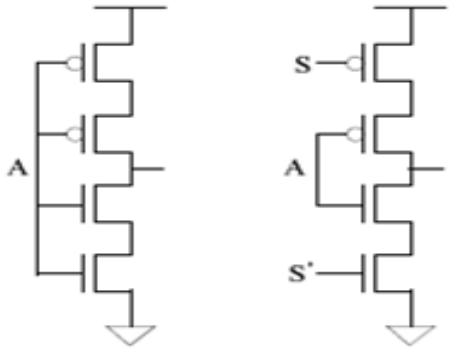

Figure: 1 (a) Forced stack inverter (left) and (b) Sleep transistor inverter (right)

IV. LOW LEAKAGE STRUCTURE

we explain the forced stack and the sleep transistor inverters here for the purposes of comparison with a low leakage inverter. Figure 1(a) depicts a forced stack inverter, and Figure 1(b) depicts a sleep transistor inverter. The forced stack inverter breaks existing transistors into two transistors and forces a stack structure to take advantage of the stack effect; this is shown in Figure. Meanwhile, the sleep transistor inverter shown in Figure 1(b) isolates existing logic networks using sleep transistors. The stack structure in Figure 1(b) saves leakage power consumption during sleep mode. This sleep transistor technique frequently uses high-Vth sleep transistors (the transistors controlled by S and S0) to achieve larger leakage power reduction.

The low leakage technique has a structure merging the forced stack technique and the sleep transistor technique. Figure 2 shows a low leakage inverter. The low leakage

technique divides existing transistors into two transistors each typically with the same width W1 half the size of the original single transistor's width W0 (i.e., W1 = W0/2), thus maintaining equivalent input capacitance. The low leakage inverter in Figure 2(a) uses W/L = 3 for the pull-up transistors and W/L = 1.5 for the pull-down transistors, while a conventional inverter with the same input capacitance would use W/L = 6 for the pull-up transistor and W/L = 3 for the pull-down transistor (assuming μn = 2μp).

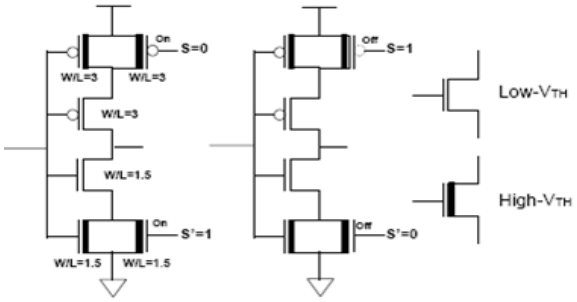

Figure: 2 (a) Low leakage active mode (left) and (b) Sleep mode (right)

Then sleep transistors are added in parallel to one of the transistors in each set of two stacked transistors. We use half size transistor width of the original transistor (i.e., we use $W_0/2$) for the sleep transistor width of the low leakage. Although we use $W_0/2$ for the width of the sleep transistor, changing the sleep transistor width may provide additional tradeoffs between delay, power and area.

V. LOW LEAKAGE OPERATION

Now we explain how the low leakage works during active mode and during sleep mode. Also, we explain leakage power saving using the low leakage structure. The sleep transistors of the low leakage operate similar to the sleep transistors used in the sleep transistor technique in which sleep transistors are turned on during active mode and turned off during sleep mode. Figure 2 depicts the low leakage operation using a low leakage inverter. During active mode (Figure 2(a)), S = 0 and S0 = 1 are asserted, and thus all sleep transistors are turned on. This low leakage structure can potentially reduce circuit delay in two ways. First, since the sleep transistors are always on during active mode, the low leakage structure achieves faster switching time than the forced stack structure; specifically, in Figure 2(a), at each sleep transistor drain, the voltage value connected to the sleep transistor source is always ready and available at the sleep transistor drain, and thus current flow is immediately available to the low-Vth transistors connected to the gate output regardless of the status of each transistor in parallel to the sleep transistors. Furthermore, we can use high-Vth transistors (which are slow but 1000X or so less leaky), for the sleep transistors and the transistors parallel to the sleep transistors without incurring large delay increase.

During sleep mode (Figure 2(b)), S = 1 and S0 = 0 are asserted, and so both of the sleep transistors are turned off. Although the sleep transistors are turned off, the sleepy stack structure maintains exact logic state. The leakage reduction of the low leakage structure occurs in two ways. First, leakage power is suppressed by high-Vth transistors, which are applied to the sleep transistors and the transistors parallel to the sleep transistors. Second, two stacked and turned off transistors induce the stack effect, which also suppresses leakage power consumption. By combining these two effects, the sleepy stack structure achieves ultra-low leakage power consumption during sleep mode while retaining exact logic state. The price for this, however, is increased area.

VI. EXPERIMENTAL METHODOLOGY

Schematics for all models and approaches are created in TANNER SEDIT Net lists are extracted from the schematic using T-SPICE. These netlists are augmented with parameters extracted from the Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm process, as well as those of the Berkeley Predictive Technology Model (BPTM) [9] 0.18, 0.13, 0.10 and 0.07 μm processes.

VII. TEST CIRCUITS

A chain of three inverters is chosen as the most basic of logic gates and is indicative of single transistor level behavior and effectiveness.

(A) THREE INVERTER CHAIN

Three inverters, equally sized (NMOS W/L = 3, PMOS W/L = 6 for the base case) are connected in series as shown in Figure 1. Measurements are made across the

inverter chain; from the first inverter's input to the last inverter's output.

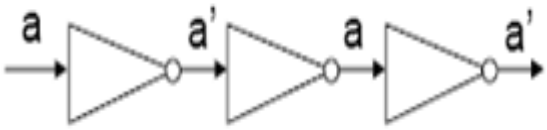

Figure: 3 Three Chain Inverter

1. DELAY

A square wave is set as input signal for the 3-inverter chain. After four periods, the delay between the input and inverted output is measured.

1. PROPAGATION DELAY

Static power for the inverter is measured by asserting high and low dc signals and averaging the power dissipated by each input after a period of 20 ns.

2. DYNAMIC POWER

Dynamic power for the inverter is measured by asserting the same square wave used in delay assessment (Section 5.1.a.) to the inverter chain input. Again, the average power dissipated over a period of 20ns is recorded as the Dynamic power of the 3 inverter chain.

TSMC 0.18µ	Propagation Delay (s)	Static Power (W)	Dynamic Power(W)
Base case	9.56E-11	4.50E-11	3.16E-06
Stack	2.46E-10	8.99E-12	3.20E-06
Sleep	1.56E-10	1.44E-11	4.79E-06
Zig Zag	1.34E-10	5.63E-12	5.43E-06
Sleepy Stack	1.78E-10	1.64E-11	3.46E-06
Sleep Dual(Vth)	2.22e-10	1.09E-12	4.56E-06
Zig Zag Dual(Vth)	1.76E-10	1.06E-17	5.21E-06
Sleepy Stack Dual(Vth)	2.19E-10	5.96E-16	3.18E-06

VIII. RESULT

1. PROPAGATION DELAY

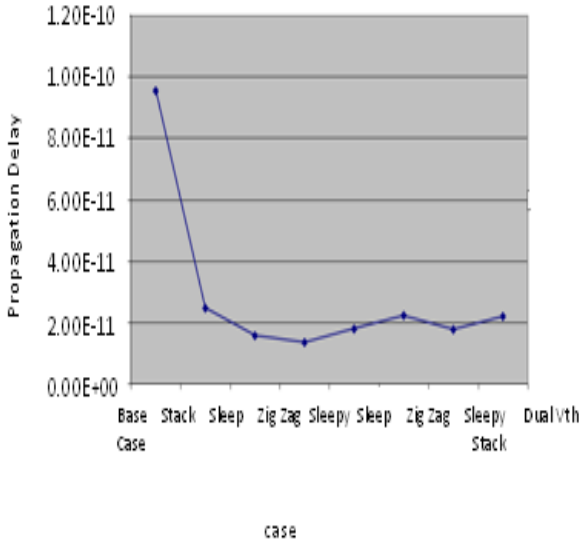

Figure: 4 Propagation delay vs case

2. STATIC POWER

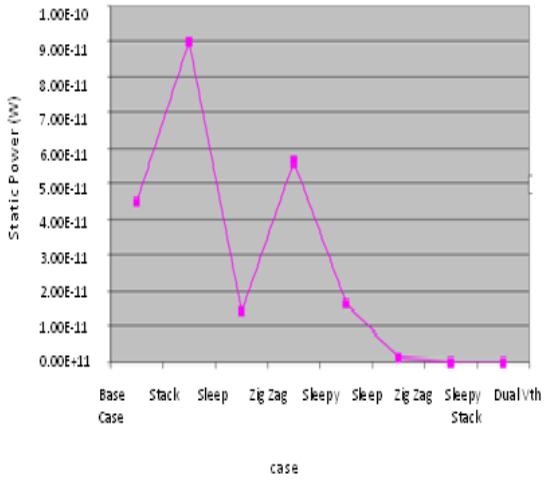

Figure: 5 Static power vs case

3. DYNAMIC POWER

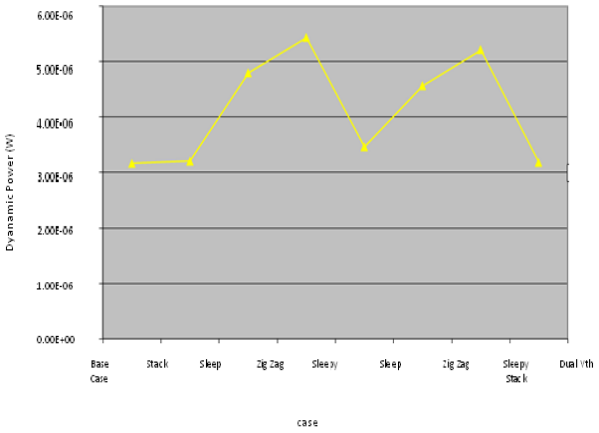

Figure: 6 Dyanamic power vs case

IX. CONCLUSION

In nanometer scale CMOS technology, sub threshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge. In this dissertation, we present a new circuit structure named "low leakage" to tackle the leakage problem. The low leakage has a combined structure of two well-known low leakage techniques, which are the forced stack and sleep transistor techniques. However, unlike the forced stack technique, the low leakage technique can utilize high-Vth transistors without incurring large delay overhead. Also, unlike the sleep transistor technique, the low leakage technique can retain exact logic state while achieving similar leakage power savings. In short, our low leakage structure achieves ultra-low leakage power consumption while retaining state.

REFERENCES

[1]. International Technology Roadmap for Semiconductors by semiconductor Industry Association, 2002. [Online]. Available http://public.itrs.net.

[2]. kim, n., austin, t., baauw, d., mudge, t., flautner, k., hu, j., irwin, m., kandemir, m., and narayanan, v., "leakage current: oore's law meets static power," ieee computer, vol. 36, pp. 68–75, december 2003.

[3]. chandrakasan, a. p., sheng, s., and brodersen, r. w., "low-power cmos digital design," ieee journal of solid-state circuits, vol. 27, no. 4, pp. 473–484, april 1992.

[4]. khellah, m. m. and elmasry, m. i., "powerminimization of high-performance submicron cmos circuits using a dual-vdd dual-vth (dvdv) approach," proceedings of the international symposium on low power electronics and design, pp. 106–108, 1999

[5]. sakurai, t. and newton, a. r., "alpha-power law mosfet model and its application to cmos inverter Delay and Other Formulas," IEEE Journal of Solid State Circuits, vol. 25, no. 2, pp. 584–593, April 1990.

[6]. bowman, k. a., austin, b. l., eble, j. c., tang, x., and meindl, j. d., "a Physical Alpha-Power Law MOSFET Model," IEEE Journal of Solid-State Circuits, vol. 34, no. 10, pp. 1410–1414, October 1999.

[7]. mutoh, s., douseki, t., matsuya, y., aoki, t., shigematsu, s., and yamada, ., "1-v power supply high-speed Digital Circuit Technology with Multithreshold-Voltage CMOS," IEEE Journal of Solis-State Circuits, vol. 30, no. 8, pp. 847–854, August 1995.

[8]. min, k.-s., kawaguchi, h., and sakurai, t., "zigzag super cut-off cmos (zsccmos) block activation with Self-Adaptive Voltage Level Controller: An Alternative to Clock-gating Scheme in Leakage Dominant Era," IEEE International Solid-State Circuits Conference, vol. 1, pp. 400–401, February 2003.