International Journal of Scientific Engineering and Technology (ISSN : 2277-1581)
Volume No.2, Issue No.6, pp : 550-553 1 June 2013

Area Efficient 4-Input Decimal Adder Using CSA and CLA

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Abstract :- ***In Today we need exact results in our computation commercial application decimal arithmetic in their computation program it takes lot of time by software support we get results but system become slower so in this paper an area efficient 4-input decimal adder using CSA and CLA is proposed to give hardware support for decimal arithmetic synthesis shows that it reduces on chip area and consume less power with same propagation delay then previously proposed adder. It could perform complex addition as per our requirement.***

Keywords :- VLSI design, Carry look ahead adder, Carry save adder, Parallel prefix adder, Decimal addition, Computer arithmetic.

1. Introduction :-

In past decades binary arithmetic is mostly used as a default base in all computers and processors why because the storage and speed efficiency But now a day's decimal arithmetic is used in our arithmetic and human being are also habitual for decimal data. We use decimal arithmetic for some reason as follows First, binary numbers cannot be represented in decimal arithmetic exactly ex.

$(0.9)_{10}=(0.1110\text{---})_2$ it cannot represent exactly it require infinite bits for representation so we use approximation but approximation gives error in output so we never get exact output.

Second Financial database contain decimal data if we are using binary hardware then first decimal data is converted into binary and after computation result which is in binary from it again convert in decimal data these conversion will increase the propagation delay.

To overcome these problems these are two method one is to provide software support for addition by software implementation of decimal arithmetic we can get exact result but it has some speed limitations. It is approximate 100 times slower then hardware support of decimal arithmetic.

Secondly we can use BCD(binary coded decimal) numbers to represent decimal no's. It is a 4-bitcode and each decimal digit can be represented in 4-bit valid BCD no's are from 0 to 9 that is $(0000)_2$ to $(1001)_2$ so $(0.9)_{10} = (0.1001)_2$ we get finite and exact representation But when two valid BCD no. are added and result is greater then g then we need to use correction logic which add $(0110)_2$ in each nibble(combination of u bit) of result so in this paper and area efficient 4-input decimal adder is proposed to give hardware support for decimal arithmetic. It can reduce chip area and consume less power with same propagation delay then previously proposed adder. This adder is proposed for fast addition.

The remainder of this paper is originated is follow In section(2) gives brief ideas about conventional decimal adder and reduced delay BCD adder. In Section(3) the area efficient 4-input decimal adder is presented section (4) define implementation result and comparision.

2. Previous Work

(a) Conventional BCD Adder

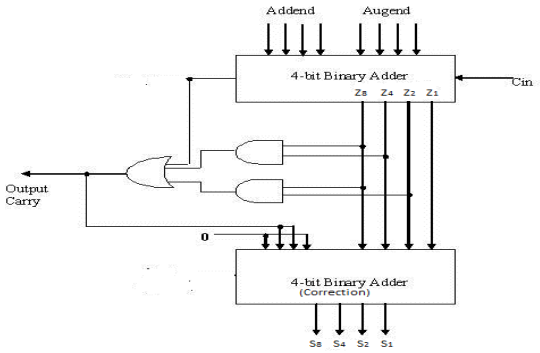

Fig. 1 Block diagram of BCD adder

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Consider two input A(Augend) and B(Addend) are given to decimal BCD adder architecture of BCD adder is shown in fig(1) further 4 full adder circuits are used to sum up A and B and if result is more then 9 then by using correction network we can add $(0110)_2$ in each nibble. 4 full adder are also used to implement correction network the correction value determined by following equation

$$C=K+Z8.Z4+Z8.Z2$$

+ define logical OR

. define logical AND

If the input bits are increased the number of full adder are also increased so the propagation delay is increased.So another reduced delay BCD adder is proposed for fast calculation.

(b) Reduced Delay BCD Adder

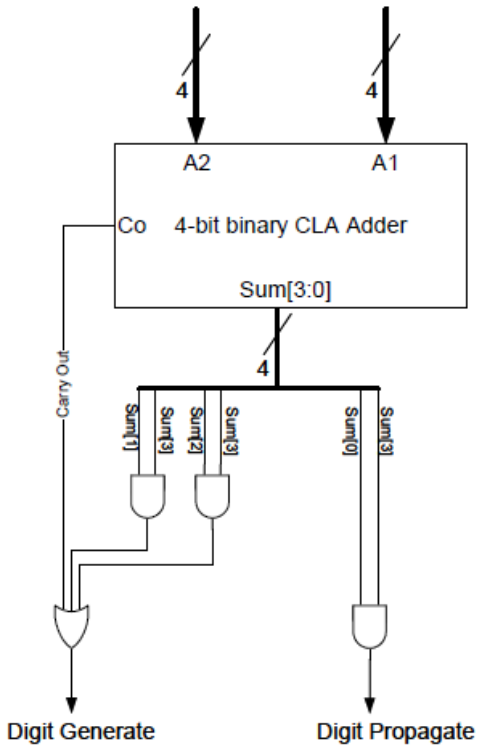

Fig 2 Adder + Analyzer

There are three stages in this adder first stage is adder + analyzer it takes two inputs and generate sum using carry look ahead adder there are two signal which is DP(Digit Propagate) and DG(Digit Generate). When the sum of two valid BCD numbers is greater then 9 this condition is identified by DG. When the sum of two BCD numbers is 9 this condition is identified by DP. DG and DP signals are sent to carry network which is composed by parallel prefix adder to generate the decimal carry.

Output carry=DG+DP.input carry

And stage 3 is correction stage which parallely added the(0110) as per requirement.

In reduced delay BCD adder, propagation delay is reduced, but on chip consumed area is increased due to carry network and an analyzer.

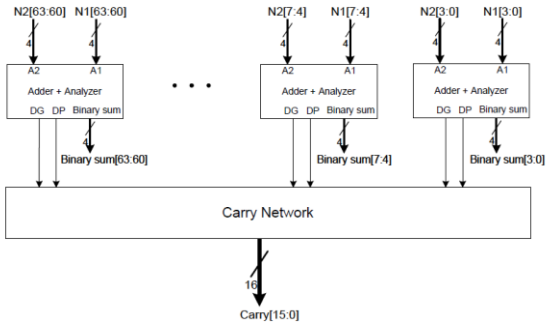

Fig. 3 Reduced delay BCD adder

3 .Area efficient 4-input decimal adder

Proposed decimal adder consist Three stages. Each input is divided into 4 digit and sent to CSA + PG network. It enerates oral sum and DG, DP signals. By using carry network we will get real sum by adding oral sum, carries, DG and DP signals. The carry network uses the concept of parallel prefix adder to increase the parallelism by which the speed of computation will increase.

In this adder, at first we need to generate sum and carries, the four inputs(each of 4 digits) send to CSA which generate sum, carries and the signals. To indicate the condition stated below,

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Digit generate signals identifies the condition if sum is greater than 9 or 19 or 29.

Digit propagate signals identify the condition if sum is equal to 7,8,9,17,18,19,27,28 or 29. The decimal carry inns may be equal to 0,1,2 or 3, it depends on the carry outs from the lower digits.

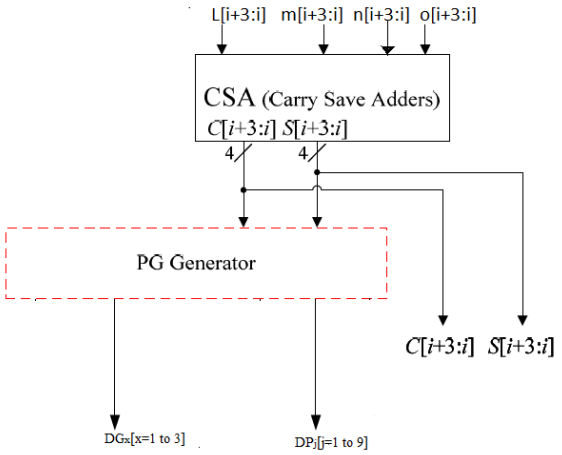

Fig. 4 CSA+PG Generator Circuit

Table 1. digit generation and propagation signals for identifying the condition of sum in each digit

Signals	Condition of the sum in each digit
DG1	>9
DG2	>19
DG3	>29
DP1	=7
DP2	=8
DP3	=9
DP4	=17
DP5	=18
DP6	=19
DP7	=27
DP8	=28
DP9	=29

Let's take a numerical example

7823

9526

3214

2413

22976

Adder and Analyzer:-

Digit 4	Digit 3	Digit 2	Digit 1
0111	1000	0010	0011
1001	0101	0010	0110
0011	0010	0001	0100
0010	0100	0001	0011
1111	1011	0000	0010
00110	01000	00110	01110

Output:-

1111	1011	0000	0010
00110	01000	00110	01110
1101	0110	0001	1110
0010 0010	1001	0111	0110

4. Conclusion

Proposed area efficient four input(each having 4 digits) adder using CSA and CLA is coded by using VHDL. This adder presents minimum delay compare to previous adder and it acquire less chip area and power consumption is also lesser than other adder by using power prime. This adder can perform addition for multiple input cases so we can obtain its generalized form.

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