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Comparative Analysis of Transimpedance Amplifier of 45 nm and 180nm CMOS Technology

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Abstract — ***This paper gives a comparative analysis of an inductorless Complementary Metal Oxide Semiconductor (CMOS) Single-ended current-mode Transimpedance Amplifier (TIA) intended for use in front-end Optical communication for wideband operation. This technique uses N similar TIAs in parallel configuration to boost the overall bandwidth as well as the transimpedance gain which is not possible with voltage-mode circuits. Using this method, we achieved the high bandwidth with high transimpedance gain, with the minimum power consumption of 64.5 and 1.6 mW for a 45 nm and 180 nm CMOS digital process respectively.***

Keywords—Current-mode, inductorless, Transimpedance amplifier (TIA), Power Consumption, Bandwidth enhancement.

I. Introduction

The intrachip interconnections uses the parallel optical links to provide low power dissipation and high-bandwidth operation [iii], [iv], [xv]. The CMOS implementation of optical transceivers is useful because both can be integrated in the same chip as the digital processing units, resulting in lower cost and power consumption. The preamplifier block of a front-end optical communication has great challenge for designing. The merits of Transimpedance amplifier (TIA) have relatively low noise and large bandwidth, which is the first gain stage and one of the essential blocks in an optical receiver. Due to the existence of high-impedance nodes, the demerits of voltage-mode circuits has limited bandwidth with high supply voltage, cannot be avoided. It is advantageous to amplify the current directly by using CMOS current-mode circuits which have many advantages over voltage-mode circuits including wide bandwidth, low supply voltage requirement, tunable input impedances, high slew rates, and less susceptible to power and ground fluctuations. These unique characteristics make current-mode circuits particularly attractive for multi-Gbps data communications [xv].

Typically, the current-mode TIA topology uses the current mirror, for the input stage to sustain small input impedance and high bandwidth. The current mode TIA topology shown in Fig.1 is useful for wide bandwidth TIA design since stability is not an issue [i]. For the current-mode TIA, the presented circuit uses a wideband CGFB topology coupled to a current-to-voltage conversion stage, and two common-source (CS) gain stages. We show that the CGFB mirror can improve bandwidth as well as transimpedance gain, reduce power consumption [i], [xv]. The design of a wideband TIA is challenging mainly because of the high capacitance of the photodetector which is ranging from 0.2 to 0.5 pF, which creates the dominant pole of the TIA and hence limits its bandwidth. The Capacitive and Inductive peaking is widely used to enhance the TIA bandwidth and makes it possible to reach a data rate of 10 Gb/s and higher in CMOS [v], [vii], [viii], [xiv] and BiCMOS [xiii]. Using inductors to increase the bandwidth of TIA has important drawbacks: 1) the chip size dramatically increases; 2) substrate coupling increases through the inductors, resulting in higher crosstalk; and 3) the TIA performance degrades in a digital process with thin metals and lossy passive components [ii], [xv]. In parallel optical links, several TIAs and photodetectors are used in parallel to create multiple channels and boost the overall data rate at the receiver [vi], [xv].

This paper, we make a comparative analysis of TIA for 180 nm [xv] and scale down for 45 nm techniques to boost the TIA bandwidth as well as transimpedance gain of the current-mode without using any inductor for interconnection. As a proof of concept, we design and implement a single-ended inductorless TIA in a digital 45 nm and 180 nm [xv] CMOS process. The single-ended current-mode TIA provides a transimpedance gain of 59 dBΩ with 8.1 GHz bandwidth and 92 dBΩ with 6.3 GHz bandwidth, for 45nm and 180 nm, respectively.

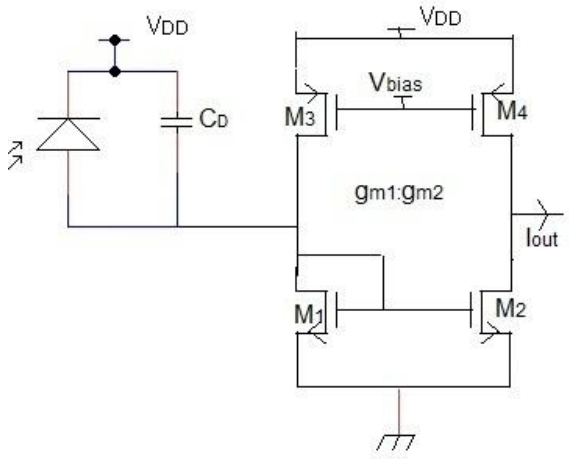

Fig. 1 TIA Current-mode topology

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II. Material and Methodology

Fig. 2 shows a Single-ended feedback TIA [ii]. R_f is the feedback resistor, C_D is the photodiode capacitance, and C_I is the voltage amplifier input capacitance. A(s) is the transfer function of the voltage amplifier for a single pole, we can write it as,

$$A(s) = \frac{-A_0}{1+{}^{s}/_{w_0}} \qquad (1)$$

The low-frequency transimpedance gain of the TIA Z_T is,

$$Z_T = \frac{A_0}{A_{0+1}} R_f \qquad (2)$$

We propose the inductorless TIA topology in Fig. 3 to increase the gain–bandwidth product [ii], [ix]. N copies of the same feedback TIA in Fig. 2 are connected together in parallel, and their output voltages are added. The transfer function of the parallel TIA in Fig. 2 with N parallel feedback TIAs is,

$$\frac{V_{out}}{I_{in}} = \frac{\frac{-A_0}{A_{0+1}} R_f w_n'^2}{s^2 + 2\tau' w'_n s + w'^2_n} \qquad (3)$$

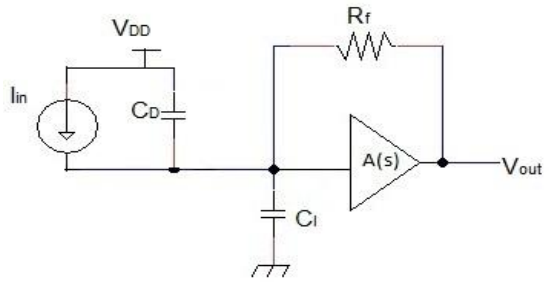

Fig. 2 Regular feedback TIA

It is evident from (3) that the dc transimpedance gain Z_T is the same as the one for the individual feedback TIA, i.e.

$$Z'_T = Z_T = \frac{A_0}{A_{0+1}} R_f \qquad (4)$$

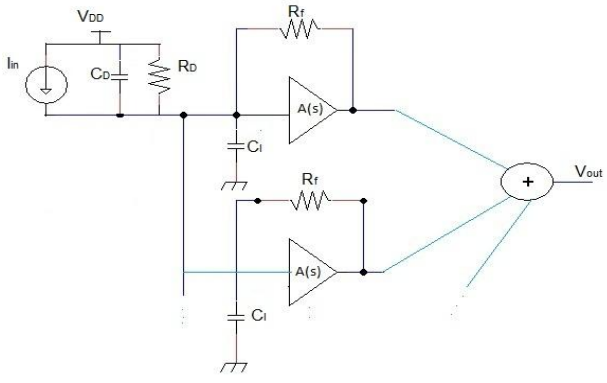

Fig. 3 TIA cascading topology

We can redraw Fig. 3 and replace C_D with C_D/N and I_{in} with I_{in}/N at the input of each feedback TIA by having R_D is of value 1 GΩ. Now, we have N TIAs that are operating independently, and each has a photodetector capacitance of N times smaller than the feedback TIA in Fig. 2. This increases the gain and bandwidth of the individual feedback TIAs. As the number of parallel feedback TIAs increases, the bandwidth increases, but, at the same time, damping factor decreases from the critical damping value of 0.7 [ii]. We choose N = 2 for this design, from Fig. 3 it results in the highest ratio of the bandwidth enhancement and the power consumption. For the first stage of the TIA, two feedback TIAs with a feedback resistor of 1KΩ are used in parallel as shown in circuit schematic in Fig. [i], [ii]. Current-mode circuits are commonly implement with current mirrors when relatively small input impedance and high bandwidth are needed [i]. The problem of high power consumption and large parasitic capacitances in current mirror is overcome by an additional branch made with a complementary transistor pair is added to the basic current mirror, leading to the CGFB topology as shown in Fig. 4 which effectively reduce the input impedance [i], [xi]. The bandwidth of the CGFB mirror is approximately two times that of the basic current mirror. The resistor R_1 of value 40 Ω, is for additional power savings [xv].

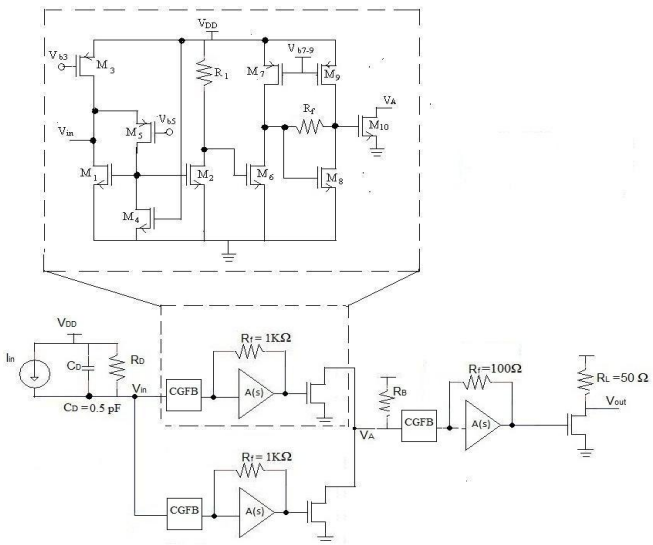

Fig. 4 Implemented TIA Block diagram and Circuit schematic

For small R_f of value 1 KΩ, the Miller amplification of the capacitance has little effect upon the bandwidth [i]. The common source buffer, M_{10} transistor of width of 25 μm is used to add the output signals from the two feedback TIAs. The second stage of the TIA is implemented using the same feedback TIA with a feedback resistor of 100 Ω. The currents by buffers are added up at node V_A and directed into the feedback TIA of the second stage. The buffer at the second stage delivers the amplified signal to a 50 Ω load.

The resistor R_B of 10K is used to bias the buffer transistors M_{10} [ii].

III. Results and Tables

The single-ended TIA in Fig. 4 was implemented in a digital 45 nm and 180 nm [xv] CMOS process. The Fig.5 shows the simulated results using 45 nm CMOS by using the value of Table I of transimpedance gains for N=1 and N=2 of the TIA in HSPICE. The simulated bandwidth and single-ended dc transimpedance gain are 8.1 GHz and 59 dBΩ, respectively, for N=2 as well as 2.9 GHz and 56 dBΩ, respectively, for N=1. The Fig.5 shows the simulated results using 180 nm CMOS [xv].

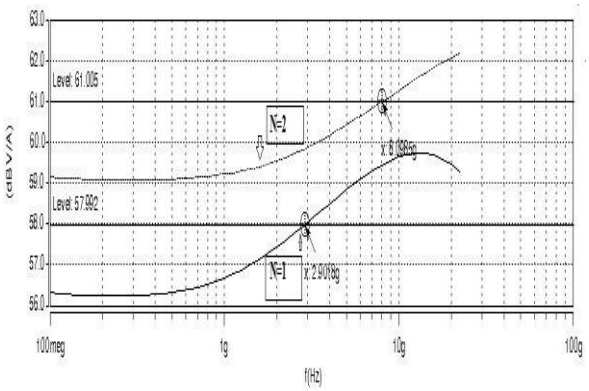

Fig. 5 Transimpedance gain (dBΩ) verses Frequency (Hz) for 45 nm CMOS

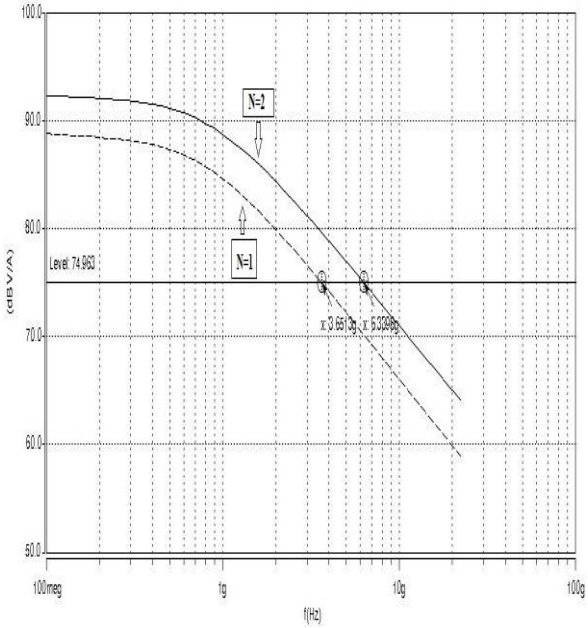

Fig. 6 Transimpedance gain (dBΩ) verses Frequency (Hz) for 180 nm CMOS [xv]

The overall input referred noise is given by,

$$\overline{I_{n,in,avg}}^2 = \frac{2\pi KT}{R_L} \quad (5)$$

The overall input referred noise is 29.4 pA/√Hz over the whole Bandwidth with photodiode capacitance and induced current of 0.5 pF and 100 nA, respectively. It consumes 64.5 mW and 1.6 mW dc power, from a 1.8V supply, for 45 nm and 180 nm, respectively. The comparative chart is shown in Table II.

TABLE I

TRANSISTOR ASPECT RATIOS (W/L)	
Transistor	***Aspect Ratio(μm/ μm)***
M_1	277.8
M_2	1388.8
M_3	166.6
M_4	10
M_5	666.6
M_6	57.3
M_7	355.5
M_8	61.1
M_9	305.5
M_{10}	555.5

TABLE II

Parameters	**Comparision with Different TIA**			
	This work	***Ref.15***	***Ref. 1***	***Ref.2***
Z_T (dBΩ)	92	59	83	62
BW (GHz)	4.7	7.97	0.115	6
D C p o w e r (mW)	1.6	60	28.6	98
Input current noise (pA/√Hz)	29.4	29.4	53n	20
Power supply (V)	1.8	1.8	1.8	2.0
Topology	Single-end	Single-end	Single-end	Diff.
Process (CMOS) nm	180	45	180	130
BW Enhancement Technique	Inductorless	Inductorless	-	Inductorless

IV. Conclusion

We have introduced a technique to boost the TIA's gain-bandwidth product without using any inductor with the latest technology 45 nm CMOS. It consumes more power comparatively with the 180 nm CMOS, but improves the bandwidth. So, it can be used in high speed parallel optical links for intrachip interconnections.

Acknowledgement

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