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Design and Implementation of Low Power Phase Frequency Detector (PFD) for PLL

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ABSTRACT— This paper presents a novel Phase frequency detector for Charge Pump Phase locked loop (PLL) applications to enable fast frequency acquisition in the phase-locked loop (PLL). To cope with the missing edge problem, the proposed PFD predicts the reset signal and blocks the corresponding input signal during the reset time. The blocked edge is regenerated after the reset signal is deactivated [1]. The PFD will be implemented using 0.18 µm technology. The designed PFD can be used in PLL with Frequency up to 1.5GHz. The results reported in this paper based on simulation done using Cadence Assura layout tool.

Key Words: Low power, Phase frequency detector (PFD), phase locked loop (PLL), Cadence, Assura.

I.INTRODUCTION

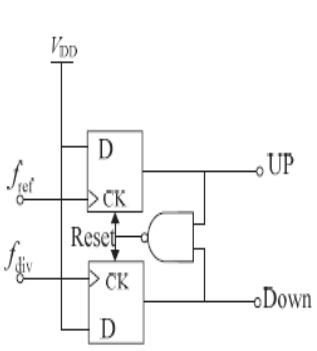
In recent years, the design of low power and low jitter PLL for the different application has become one of the greatest challenges in high-performance very large scale integration (VLSI) design. As a consequence, many techniques have been introduced to minimize the power consumption and reduction in jitter of new VLSI circuits. Phase locked loop (PLL) is a main block in many applications such as wireless communication systems, digital circuits, and sensor's receivers [3]. It is a clock or carrier generator. These applications need low power blocks to have long life battery. Phase Frequency Detector (PFD) is one of the PLL blocks. The main concept of PFD is comparing two input frequencies in terms of both phase and frequency [7]. In a PLL the two frequencies are reference frequency (Fref) and the voltage controlled oscillator (VCO) output after division by N (Fvco) [4]. A PFD is usually built using a state machine with memory element such as D flip-flop. There are many topologies moving towards simplifying the circuit and reducing the dead zone. Dead zone is a main property in the PFD phase characteristics as it introduces jitter to the PLL system [8]. The PFD doesn't detect the phase error when it is within the dead zone region, then PLL locks to a wrong phase [3].

The paper is organized as follows:

The design of proposed PFD circuit is explained in section II. Phase characteristics and frequency characteristics are discussed in sections III and IV respectively Simulation results are in section V. The conclusion is in section VI.

II. DESIGN OF PROPOSED PFD CIRCUIT

Fig.1 illustrates a common linear PFD architecture using two DFFs and a NAND gate [2, 3]. The DFFs are triggered by the inputs to the PFD. Initially, both outputs are low. When one of the PFD inputs rises, the corresponding output becomes high. The state is held until the second input goes high, which in turn resets the circuit and returns the PFD to the initial state. Fig. 2 illustrates the ideal characteristics of PFD [9]. From the characteristics, the input linear range is from -2π to 2π. However, due to the delay of the reset path, the linear range is usually less than 4π [5].



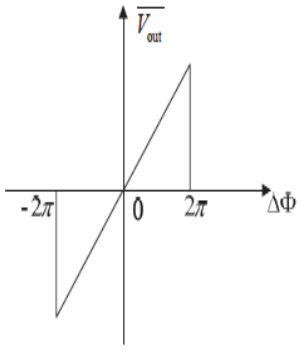


Fig (1): Common PFD Architecture Fig (2): Ideal Linear Characteristics

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A. Design of the Proposed PFD

The proposed design is shown in Fig. 4 [5]. The PFD is similar to a dynamic two-phase master–slave pass-transistor flip-flop. Only single-edge clocks are used to minimize clock skew. As both outputs become high, the slave is reset asynchronously while the master is reset synchronously, i.e., the reset is allowed only when the slave latch is transparent. Synchronously resetting the master increases the operating range and also increases the power consumption. If the master latch is reset while it is transparent, then there will be significant short-circuit current. The reset circuit shown in Fig. 4 includes one pass transistor, one inverter, and one NAND gate [4]. In order to properly reset the slave, the pass-transistor output should become high before the master becomes transparent. Hence, the NAND gate delay is counted twice in the delay path.

B. Implementation of PFD using D-flip flop pass transistor logic

The Pass Transistor D Flip Flop circuit is shown in Fig. 3. The PFD is made by two D flip flops as shown in Fig. 4. In this design synchronous reset is used for master and slave. i.e., the reset is allowed for both master and slave outputs. The operating range of the design is increased with the help of synchronous resetting and also the power consumption is reduced compared to the traditional PFD. If the master latch is reset while it is transparent, then there will be significant short-circuit current, resulting in more power consumption. The output of the PFD when Fref signal rising edge leads Fvco signal rising edge and vice versa is shown in the Fig. 6 and Fig. 7 respectively.

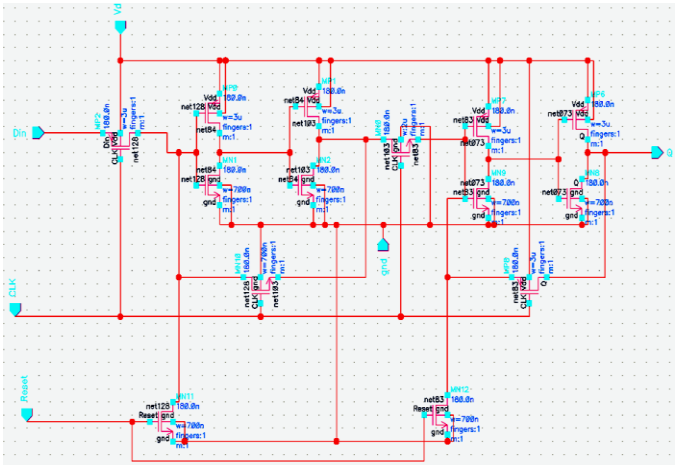

Fig (3) D Flip flop using pass transistor logic.

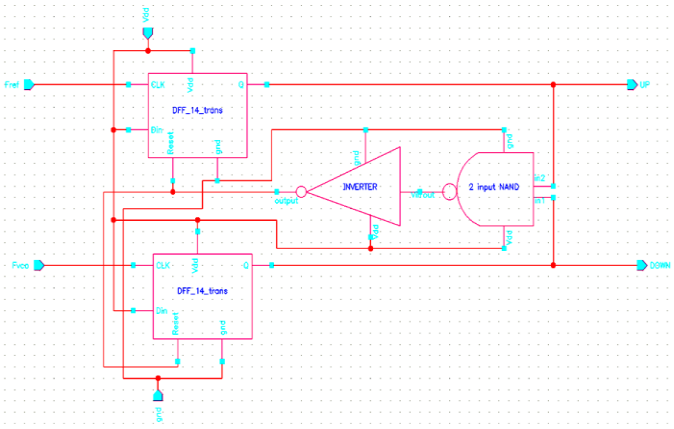

Fig (4) Phase Frequency Detector

C. *Layout Design of the Proposed PFD*

Fig.5 illustrates the layout of the proposed PFD. The layout for the D flip flop schematic shown in Fig.3. The different layers can be recognized by their colors. Yellow color represents poly silicon layer, silver color layer is metal 1 layer and red color layer is metal 2. Body contacts are connected to VDD and ground respectively. N-well is connected to all pMOS transistors. Pins are shown by cross marks.

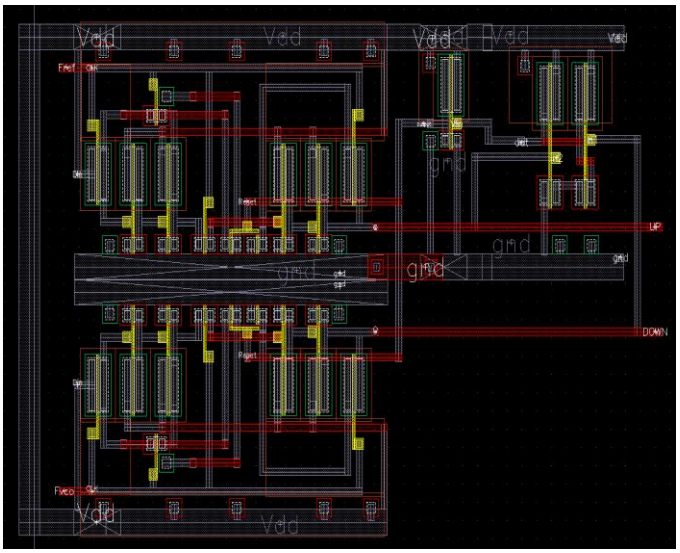

Fig (5) Layout of the PFD

IV. SIMULATION RESULTS

All simulations are done using GPDK 180nm technology. All n-channel devices have a width of 700nm, and all p-channel devices have a width of 3um. VDD is chosen to be 1.8 V for CMOS latch and BGB latch. All simulations are performed by using Cadence tool.

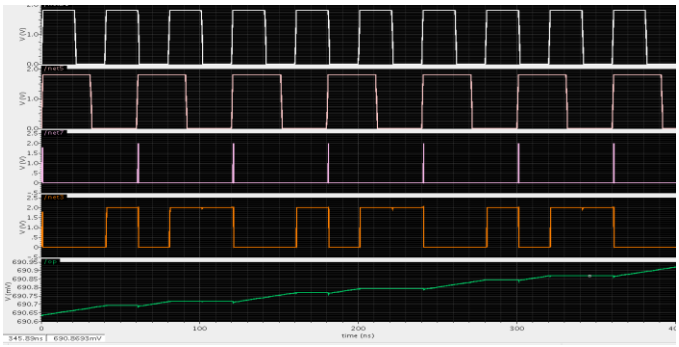

Fig (6) Fref is higher than Fvco.

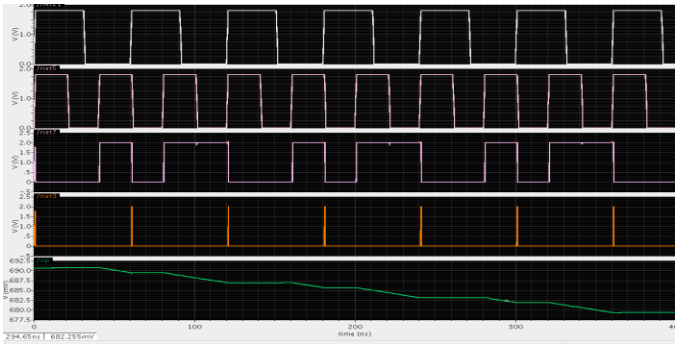

Fig (7) Fvco is higher than Fref

V. PFD'S PERFORMANCE SUMMARY

parameter	[1]	[2]	proposed
Technology	0.25µm	0.50µm	0.18µm
Operating Frequency	up to 800MHz	Up to 800Mhz	Up to 1.5GhZ
Power dissipation	--	300mW	22.38nW
VDD in volts	2.5	5	1.8

Table 1.

VI. CONCLUSION

This paper presents a new PFD design for PLL. As the missing edge reverses the output polarity of the PFD, it plays a significant role in determining the acquisition time. To achieve fast acquisition by removing the missing edge problem, a new PFD has been presented in this paper. Table 1 shows the comparison of reference paper [1], [2] and proposed design work. In the proposed PFD, the reset signal is predicted to block the corresponding input signal and the blocked edge is regenerated after the reset signal is deactivated. Experimental results show that the proposed PFD results in low power consumption, low voltage utilization and uses only 34 transistors, implemented in a 0.18µm CMOS technology.

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