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Capacitance Based Low Power ALU Design and Implementation on 28nm FPGA

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Abstract— ***In this work, capacitance and technology scaling is used for further reduction in IOs power. On 40nm technology and 10 GHz operating frequency, there is 4.59%, 9.38%, 13.97% and 18.76% reduction in IOs power when capacitance change from 5pF to 4pF, 3pF, 2pF and 1pF respectively. On 28nm technology and 10 GHz operating frequency, there is 5.54%, 11.32%, 16.86%, and 20.72% reduction in IOs power when capacitance changes from 5pF to 4pF, 3pF, 2pF and 1pF respectively. There is 17.16% and 17.99% reduction in power on 5pF and 4pF capacitance respectively on 10 GHz. There is 18.94%, 19.95% and 19.16% reduction in power on 3pF, 2pF and 1pF capacitance respectively on 10GHz. Target Device is Virtex-6 for 40nm and Artix-7 for 28nm.***

***Index Terms*—LVCMOS, IO standard, Low Power, Energy Efficient Design, Capacitance Scaling**

I. INTRODUCTION

rithmetic logic unit in extended form is taken as math Acoprocessor. It is used to solve arithmetical and logical functions. Technology scaling to 28nm is the default way to reduce dynamic power consumption of ALU. For more reduction in IOs power, we reduce capacitance because device capacitance requirements vary with CLB and I/O utilization. The transmission line charge time is dependent on the output load capacitance of the receiver and the output impedance of the driver. A real capacitor of any type then not only has capacitance characteristics but also inductance and resistance characteristics. A parasitic model of a real capacitor is shown in Figure 1.

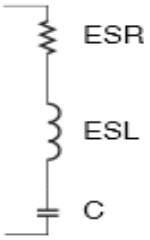

Figure 1: Parasitic of a Real, Non-Ideal Capacitor [Source: Ref7]

A real capacitor is an RLC circuit (a circuit, which has three components, first is a resistor (R), second is an inductor (L), and third is a capacitor (C), all connected in series). A shunt capacitance (as shown in Figure 2) causes a momentary dip in the impedance.

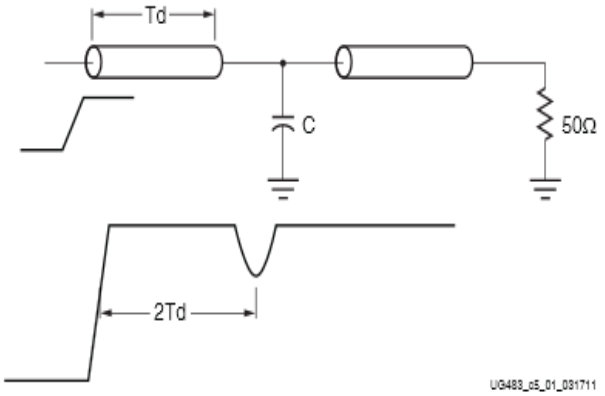

Figure 2: Shunt Capacitance for Reduction in Impedance [Source: Ref7]

$$Power = (Capaci\tan ce) * V_{DD}^2 * f$$

Power is directly proportional to Capacitance. For low power design, we try to reduce the capacitance of target design.

II. RELATED WORKS

Reference [1] addresses a synthesis process of VHDL code for FPGA design flow using Xilinx PlanAhead tool. This tool provide a low power profile, more hard IP functionality, **lower node capacitance** & architectural innovations, and synthesis frameworks. A feature like lower node capacitance is discussed in [1]. Reference [2] presents the graphene-based system application and shows the potential of graphene wires of lower capacitance for ultralow power electronics. Clock signals are responsible for a significant portion of dynamic power in FPGAs due to capacitance is discussed in [3]. Ref [4] presents the assessment of using field programmable gate arrays (FPGA) technology to design a stand-alone electrical capacitance tomography (ECT) system. Intensive image reconstruction algorithms reduce time complexity of ECT application for large amounts of data. According to reference [4], reconfigurable hardware used first time in the area of electrical tomography. And, the results show that FPGA based ECT system achieves superior performance in [4] in terms of speed and power compared to DSP implementation. Reference [5] reports design and fabrication of a low-voltage high-speed field programmable gate array (FPGA) I/O cell (IOC) IC in a commercial 90 nm CMOS technology. IOC IC in [5] supports forty common industrial I/O standards. This design features function-based I/O

standard partitioning for simpler architecture, capacitance, block sharing for smaller size and lower power dissipation. In reference [6], 35.9% dynamic power reduction and 36.11% dynamic current reduction is achieved by shifting drive strength from 24mA to 2mA on LVCMOS25 when 2.5 V is output driver supply voltage and 1.0V is input supply voltage. Reference [6] also achieve 30% dynamic power reduction and 21.7% dynamic current reduction by shifting drive strength from 24mA to 2mA on LVCMOS12 for 1.2V is output driver supply voltage and 1.0V input supply voltage. We are extending this work on resistance to capacitance for low power design because device capacitance changes with change in CLB and I/O utilization. Reference [7] is PCB Design and Pin Planning Guide of Artex-7 Series FPGAs.

III. Capacitance Scaling in ALU on 40nm

A. Power Varies with Capacitance in ALU on 100MHz

Table 1: Capacitance Scaling on 100 MHz and 40nm

	Clocks	Logic	Signals	IOs	Leakage	Total
5pF	0.000	0.000	0.000	0.005	0.711	0.716
4pF	0.000	0.000	0.000	0.005	0.711	0.716
3pF	0.000	0.000	0.000	0.005	0.711	0.716
2pF	0.000	0.000	0.000	0.004	0.711	0.715
1pF	0.000	0.000	0.000	0.004	0.711	0.715

On 100 MHz operating frequency, there is 20% reduction in IOs power when capacitance changes from 5pF to 1pF as shown in Table 1.

B. Power Varies with Capacitance in ALU on 1GHz

Table 2: Capacitance Scaling on 1 GHz and 40nm

	Clocks	Logic	Signals	IOs	Leakage	Total
5pF	0.001	0.001	0.001	0.048	0.711	0.762
4pF	0.001	0.001	0.001	0.048	0.711	0.762
3pF	0.001	0.001	0.001	0.045	0.711	0.759
2pF	0.001	0.001	0.001	0.043	0.711	0.757
1pF	0.001	0.001	0.001	0.041	0.711	0.755

On 1 GHz operating frequency, there is 6.25%, 10.41%, and 14.58% reduction in IOs power when capacitance changes from 5pF to 3pF, 2pF and 1pF respectively as listed in Table2.

C. Power Varies with Capacitance in ALU on 10GHz

Table 3: Capacitance Scaling on 10 GHz and 40nm

	Clocks	Logic	Signals	IOs	Leakage	Total
5pF	0.008	0.005	0.012	0.501	0.711	1.238
4pF	0.008	0.005	0.012	0.478	0.711	1.214
3pF	0.008	0.005	0.012	0.454	0.711	1.191
2pF	0.008	0.005	0.012	0.431	0.711	1.167
1pF	0.008	0.005	0.012	0.407	0.711	1.144

On 10 GHz operating frequency, there is 4.59%, 9.38%, 13.97% and 18.76% reduction in IOs power when capacitance change from 5pF to 4pF, 3pF, 2pF and 1pF respectively as listed in Table 3.

D. Power Varies with Capacitance in ALU on *100GHz*

Table 4: Capacitance Scaling on 100 GHz and 40nm

	Clocks	Logic	Signals	IOs	Leakage	Total
5pF	0.079	0.021	0.102	5.013	0.719	5.934
4pF	0.079	0.021	0.102	4.778	0.718	5.699
3pF	0.079	0.021	0.102	4.543	0.718	5.463
2pF	0.079	0.021	0.102	4.308	0.718	5.228
1pF	0.079	0.021	0.102	4.073	0.717	4.992

On 100 GHz operating frequency, there is 4.68%, 9.37%, 14.06% and 18.75% reduction in IOs power when capacitance change from 5pF to 4pF, 3pF, 2pF and 1pF respectively as listed in Table 4.

IV. Capacitance Scaling in ALU on 28nm

A. Power Varies with Capacitance in ALU on 100 MHz

Table 5: Capacitance Scaling on 100 MHz and 28nm

	Clocks	Logic	Signals	IOs	Leakage	Total
5pF	0.000	0.000	0.000	0.004	0.039	0.043
4pF	0.000	0.000	0.000	0.004	0.039	0.043
3pF	0.000	0.000	0.000	0.004	0.039	0.043
2pF	0.000	0.000	0.000	0.003	0.039	0.043
1pF	0.000	0.000	0.000	0.003	0.039	0.042

On 100 MHz operating frequency, there is 25% reduction in IOs power when capacitance changes from 5pF to 2pF and 1pF respectively as listed in Table 5.

B. Power Varies with Capacitance in ALU on 1 GHz

Table 6: Capacitance Scaling on 1 GHz and 28nm

	Clocks	Logic	Signals	IOs	Leakage	Total
5pF	0.001	0.001	0.001	0.042	0.039	0.083
4pF	0.001	0.001	0.001	0.039	0.039	0.081
3pF	0.001	0.001	0.001	0.037	0.039	0.079
2pF	0.001	0.001	0.001	0.034	0.039	0.076
1pF	0.001	0.001	0.001	0.032	0.039	0.075

On 1 GHz operating frequency, there is 7.14%, 11.90%, 19.04%, and 23.81% reduction in IOs power when capacitance changes from 5pF to 4pF, 3pF, 2pF and 1pF respectively as listed in Table 6.

C. Power Varies with Capacitance in ALU on 10GHz

Table 7: Capacitance Scaling on 10 GHz and 28nm

	Clocks	Logic	Signals	IOs	Leakage	Dynamic
5pF	0.008	0.005	0.010	0.415	0.039	0.477
4pF	0.008	0.005	0.010	0.392	0.039	0.453
3pF	0.008	0.005	0.010	0.368	0.039	0.430
2pF	0.008	0.005	0.010	0.345	0.039	0.406
1pF	0.008	0.005	0.010	0.329	0.039	0.383

On 10 GHz operating frequency, there is 5.54%, 11.32%, 16.86%, and 20.72% reduction in IOs power when capacitance changes from 5pF to 4pF, 3pF, 2pF and 1pF respectively as listed in Table 7.

D. Power Varies with Capacitance in ALU on *100GHz*

Table 8: Capacitance Scaling on 100 GHz and 28nm

	Clocks	Logic	Signals	IOs	Leakage	Total
5pF	0.077	0.018	0.088	4.153	0.040	4.375
4pF	0.077	0.018	0.088	3.917	0.040	4.140
3pF	0.077	0.018	0.088	3.682	0.040	3.904
2pF	0.077	0.018	0.088	3.446	0.040	3.669
1pF	0.077	0.018	0.088	3.211	0.040	3.433

On 100 GHz operating frequency, there is 5.68%, 11.34%, 17.02%, and 22.68% reduction in IOs power when capacitance changes from 5pF to 4pF, 3pF, 2pF and 1pF respectively as listed in Table 8.

E. Power Varies with Capacitance in ALU on 1THz

Table 9: Capacitance Scaling on 1 THz and 28nm

	Clocks	Logic	Signals	IOs	Leakage	Total
5pF	0.770	0.142	0.862	41.528	0.096	43.397
4pF	0.770	0.142	0.862	39.173	0.088	41.034
3pF	0.770	0.142	0.862	36.819	0.080	38.672
2pF	0.770	0.142	0.862	34.464	0.074	36.311
1pF	0.770	0.142	0.862	32.110	0.068	33.951

On 1 THz operating frequency, there is 5.67%, 11.34%, 17.01%, and 22.68% reduction in IOs power when capacitance changes from 5pF to 4pF, 3pF, 2pF and 1pF respectively as listed in Table 9.

V. Power Affected By Technology Change

A. Power on 1 GHz Device Operating Frequency

Table 10: Power Affected by Technology Change on 1GHz

	40nm	28nm
5pF	0.048	0.042
4pF	0.048	0.039
3pF	0.045	0.037
2pF	0.043	0.034
1pF	0.041	0.032

There is 12.5% and 18.75% reduction in power on 5pF and 4pF capacitance respectively on 1 GHz as shown in Table 10.

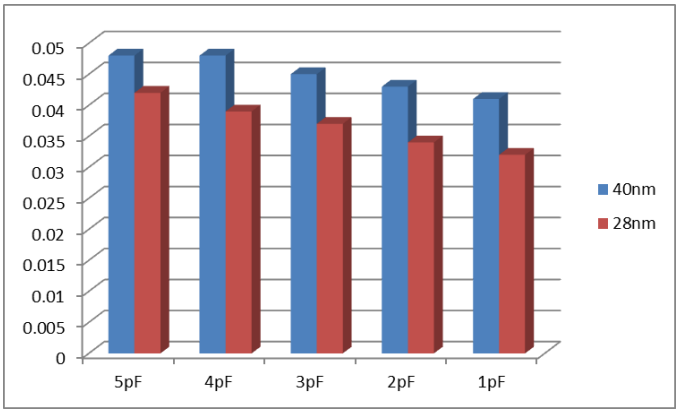

Figure 3: Power (W) varies with Different Technology and Capacitance

There is 17.78%, 20.93% and 21.95% reduction in power on 3pF, 2pF and 1pF capacitance respectively on 1 GHz as shown in Table 10.

B. Power on 10 GHz Device Operating Frequency

Table 11: Power Affected by Technology Change on 10 GHz

	40nm	28nm
5pF	0.501	0.415
4pF	0.478	0.392
3pF	0.454	0.368
2pF	0.431	0.345
1pF	0.407	0.329

There is 17.16% and 17.99% reduction in power on 5pF and 4pF capacitance respectively on 10 GHz as shown in Table 11.

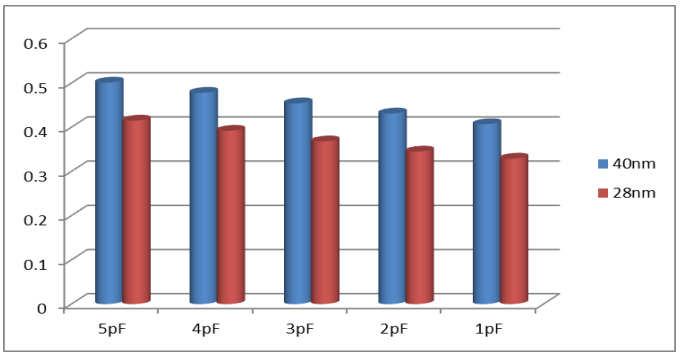

Figure 4: Power (W) varies with Different Technology and Capacitance

There is 18.94%, 19.95% and 19.16% reduction in power on 3pF, 2pF and 1pF capacitance respectively on 10GHz as shown in Table 11.

C. Power on 100 GHz Device Operating Frequency

Table 12: Power Affected by Technology Change on 100 GHz

	40nm	28nm
5pF	5.013	4.153
4pF	4.778	3.917
3pF	4.543	3.682
2pF	4.308	3.446
1pF	4.073	3.211

There is 17.16% and 18.02% reduction in power on 5pF and 4pF capacitance respectively on 100 GHz as shown in Table 12.

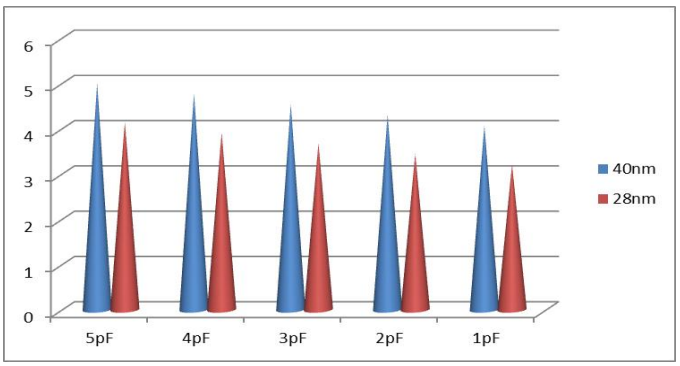

Figure 5: Power (W) varies with Different Technology and Capacitance

There is 18.95%, 20.00% and 21.16% reduction in power on 3pF, 2pF and 1pF capacitance respectively on 100 GHz as shown in Table 12.

VI. CONCLUSION

On 100 GHz operating frequency and 40nm technology, there is 4.68%, 9.37%, 14.06% and 18.75% reduction in IOs power when capacitance change from 5pF to 4pF, 3pF, 2pF and 1pF respectively. On 100 GHz operating frequency, there is 5.68%, 11.34%, 17.02%, and 22.68% reduction in IOs power when capacitance changes from 5pF to 4pF, 3pF, 2pF and 1pF respectively. There is 17.16% and 18.02% reduction in power on 5pF and 4pF capacitance respectively on 100 GHz. There is 18.95%, 20.00% and 21.16% reduction in power on 3pF, 2pF and 1pF capacitance respectively on 100 GHz.

VII. FUTURE SCOPE

This work is done for 8-bit ALU. There is open scope to design larger ALU like 16-bit ALU or even bigger 32-bit ALU or 64-bit ALU for the latest multi core processor architecture like i5 and i7.

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