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Performance of 3-Phase Neutral Point Clamped Active Front End Multilevel Converter

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ABSTRACT
For medium voltage, high power applications 3-phase neutral point clamped AC-DC multilevel converters are becoming a good choice. In this paper the performance of a 3-phase neutral point clamped Active Front End three level converter for high power application with simplified control scheme is presented. A complete mathematical model of the control scheme is developed and performance is investigated for balanced load in terms of voltage unbalance across dc link, voltage stress across the switches and THD in the line current.

Keywords: **Auxiliary circuit, Active Front End Converter, DC link capacitors, multilevel converters.**

1. Introduction

AC-DC converters are extensively used in power supplies, dc motor drives, front end converters in adjustable-speed drives, high voltage DC transmission, switch-mode power supplies, utility interface with non-conventional energy sources etc. Earlier the conversions from AC to DC were carried out by diode or phase controlled rectifier which act as non linear load on the power utility. Such non linear load draws current which is rich in harmonics with poor supply power factor, thus creating serious issue of power quality. Due to these issues regulatory agencies have issued several strict standards such as IEEE 519, IEC555 etc. to impose limits on permissible harmonic contents and reactive power drawn from supply[1-2]. To meet such strict standards, classically shunt passive filters consisting of tuned LC components and/or high pass filters are used to suppress the harmonics as well as power capacitors are employed to improve the power factor of the utility/mains. But these conventional methods have the limitations of fixed compensation, large size, and cost, and can excite resonance conditions. Active power filters have also been researched extensively to address such issues [3]. But they have the drawbacks of large rating, size, cost and complexity in control.

To overcome these drawbacks and for improved power quality, high power factor converters (HPFC) became the inherent part of AC-DC conversion. Important features of HPFCs are conversion at unity power factor with higher efficiency, reduced size and well regulated dc output [4-6]. But these high power factor converters using high voltage rating devices are having limitations such as large dv/dt, large voltage stress across switching device, large common mode voltage, high switching frequency etc. [7-10].

Due to continuous research in the field of developing efficient static power conversion, a new age of converters i.e. multilevel converters have now reached to certain level of maturity [11-13]. Multilevel structure is gaining lot of popularity because of its excellent performance in terms of sinusoidal input current with negligible harmonic contents, unity power factor, less ripple in regulated dc output voltage, reduced voltage stress across switch, reduced dv/dt and low electromagnetic interference with neighboring communication lines as compared to its counterpart 2-level HPFCs [14]. Diode-clamped multilevel converter is the most widely used topology in multilevel power conversion [7-9]. Though, it has so many advantages over its counterpart conventional 2-level converters, it suffers from serious problem of unbalance voltage of dc link capacitors under unbalanced loading conditions [15]. The voltage equalization of dc link capacitors is the necessary precondition for stable operation of a diode clamped multilevel converters [16].

The basic concept of dc link voltage balancing is to redistribute the charge through each capacitor. One way to control dc link is modifying the control technique involved. Many carrier based control techniques such as Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) [17-19] have been proposed to mitigate these problems. SVPWM control technique requires very complicated control algorithm at higher level which is difficult to implement without sophisticated and costly control platform [21]. These methods try to switch among the states having zero neutral point potential i.e. completely balanced dc link.

Another way to deal with the issue of capacitor voltage unbalance problem is the use of additional hardware circuitry such as voltage regulators, separate dc sources or additional balancing circuit [16, 22]. The problem with the auxiliary circuits used for balancing purpose is the extra cost, as well as higher switching losses. A closed loop control method which employs addition of off-set voltage signal to the reference voltage signal is given in [23]. This not only balanced the dc link but also reduced the switching losses by inserting 'no switching zone' in each half cycle of the phase voltage. A detailed switching losses investigation was carried out in [24]. Hence this problem can be dealt

effectively for better performance of multilevel converters for high power applications.

In this paper, a simplified control scheme is analyzed for 3-level rectifier under balanced and unbalanced loading condition. The adverse effects of unbalanced load for the stable operation of rectifier are highlighted with respect to voltage stress across the switches and other power quality issues. The presented concept of balancing dc link capacitor voltage is based on famous ping-pong theory [16]. The mathematical modeling of auxiliary circuit based on ping-pong theory and its working principle is presented in this paper.

The paper is organized as follows: Section II gives description of neutral point clamped multilevel AC-DC converter under balanced load and unbalanced with simplified control scheme for improved power quality in terms of input power factor, input current THD and neutral point potential variation. Section III deals with the performance analysis of neutral point clamped multilevel AC-DC converter under unbalanced load with auxiliary circuit for voltage balancing of dc link capacitors is presented by conclusion in section IV.

2. THREE PHASE THREE LEVEL NEUTRAL POINT CLAMPED AC/DC CONVERTER

2.1 Power and Control Circuit

A three-phase, three-level neutral-point clamped active front end rectifier is shown in Fig.1. There are four power switches (S_{a1}, S_{a2}, S'_{a1} and S'_{a2} for phase 'A') in one leg for each phase and each leg is clamped with clamping diodes (D_1 & D_1' for phase 'A'). Active front end rectifier is fed by 3-phase AC source connected through boost inductor (L_s). C_1 and C_2 are the dc link capacitors and midpoint of dc link capacitors and clamping diodes of each leg is connected to the neutral of three phase AC source. The load resistance R_1 and R_2 are connected across the dc link capacitors.

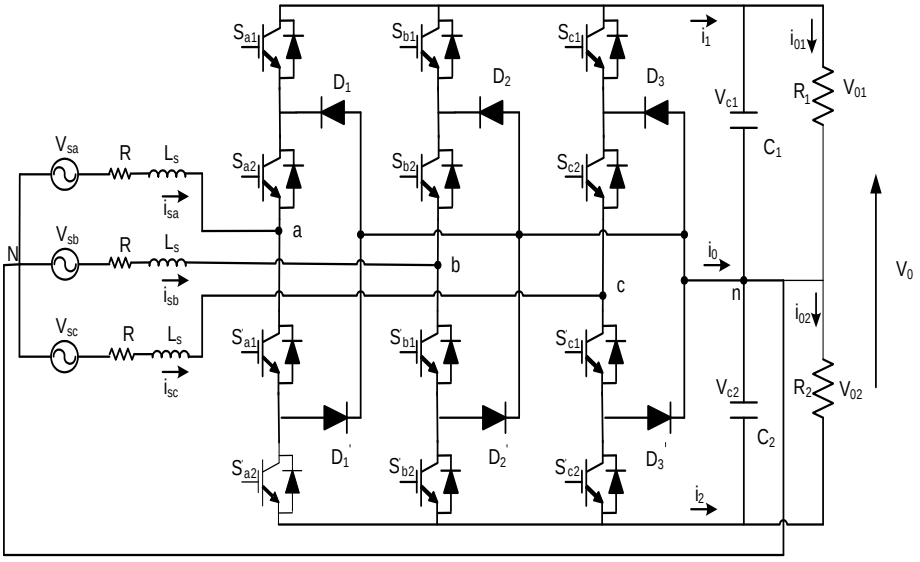

Fig.1 Three-Phase Neutral-Point Clamped Active Front End Three-Level Rectifier

Fig. 2 shows control scheme used to maintain the dc bus voltage at desired level and for improved power quality at supply side. The control scheme used consists of a voltage controller and current controller. The carrier based unipolar PWM waveforms of line-to-neutral voltages v_{an},v_{bn} and v_{cn} are produced at input side of the converter[14]. The phase locked loop (PLL) circuit is used to generate three unit sinusoidal voltages synchronized with the AC source voltages. Reference supply currents (Isa*, Isb*, Isc*) are calculated by multiplying the amplitude of the input current commands (I_m) and the generated unit sinusoidal voltages. PI controller is used to minimize the error between two dc link voltages and to generate input current command, I_m. These reference current commands are compared with actual load currents. Error generated is processed through another PI controller. Control or reference voltages are generated by comparing the output of PI controller and output of PLL. The PWM modulator is used to obtain the switching signals for the power switches by comparing these reference/control voltage signals with triangular carrier waves.

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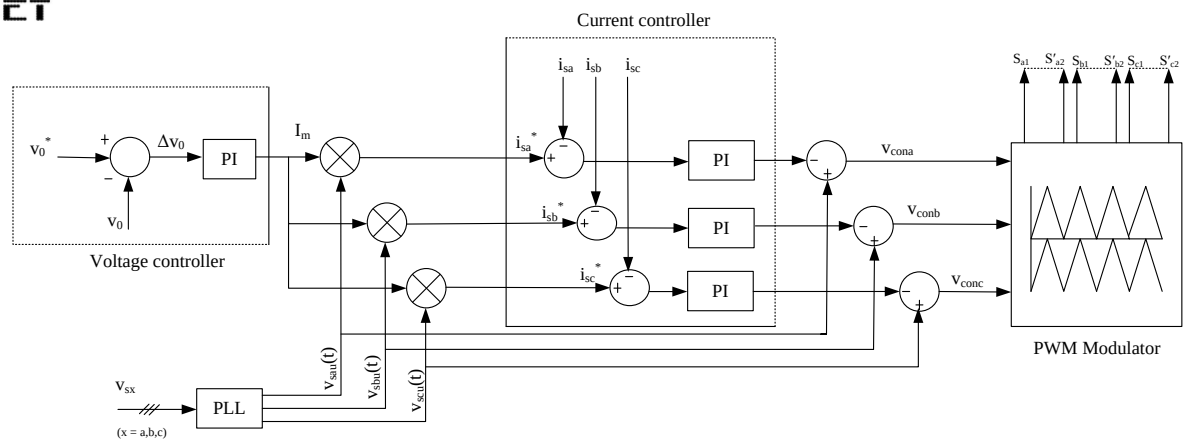


Fig.2 Schematic diagram of 3-phase, 3-level neutral point clamped multilevel rectifier control scheme.

A proportional integral voltage controller is used to balance AC side power and DC side power of the rectifier, to obtain the amplitude of the line current command i.e. I_m. The current command can be given as:

$$I_m = k_p \Delta v_0 + k_i \int \Delta v_0 \qquad (1)$$

where $\Delta v_0 = v_0^* - v_0$ is the DC bus voltage error, v_0^* is the reference DC link voltage command and v_0 is the measured DC link voltage. The unit sinusoidal voltages generated through PLL can be written as:

$$\left.\begin{aligned} v_{sau}(t) &= \sin \omega t \\ v_{sbu(t)} &= \sin(\omega t + 2\pi/3) \\ v_{scu(t)} &= \sin(\omega t - 2\pi/3) \end{aligned}\right\} \qquad (2)$$

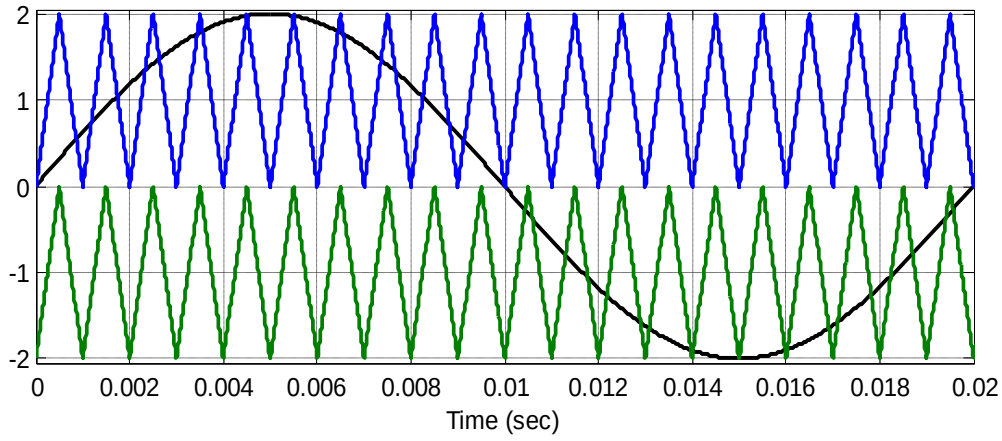
The line current commands are derived from the multiplication of the output of the voltage controller and the unit sinusoidal voltages as:

$$\left.\begin{aligned} i_a^*(t) &= I_m \sin(\omega t) \\ i_b^*(t) &= I_m \sin\left(\omega t - 2\pi/3\right) \\ i_c^*(t) &= I_m \sin\left(\omega t + 2\pi/3\right) \end{aligned}\right\} \qquad (3)$$

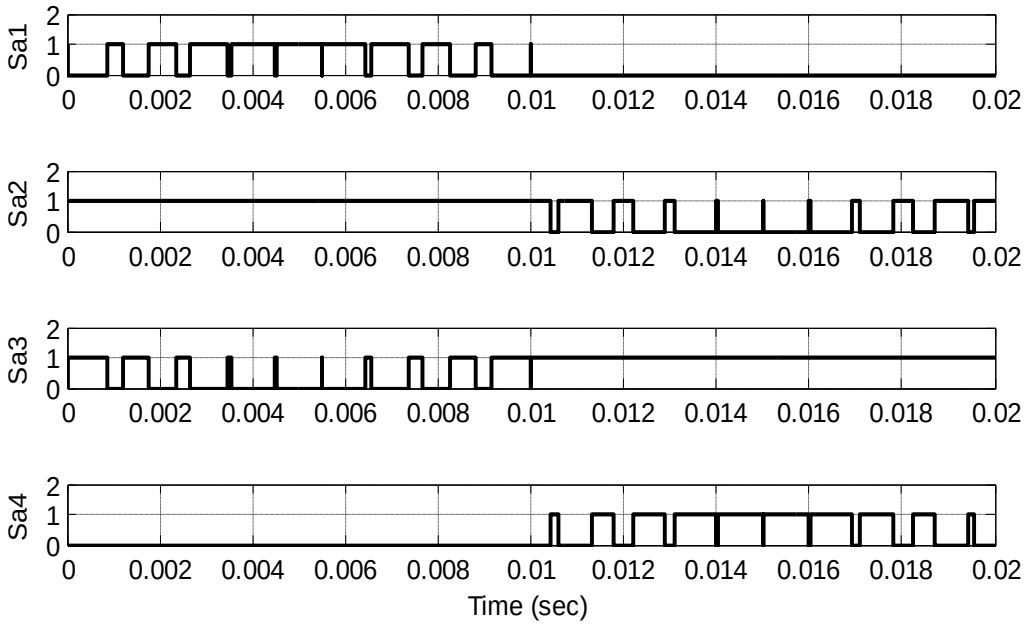
The measured line currents are compared with the respective reference line currents and the current errors thus generated are fed to the current controller to track the source current commands. Neglecting the high-frequency switching terms, we can write source voltage of phase 'A' as,

$$v_{sa} = L_{sa} \frac{di_{sa}}{dt} + v_{cona} \qquad (4)$$

where v_{cona} is the modulated control/reference voltage signal of PWM modulator derived from the proposed closed loop control of the system. The carrier-based sinusoidal PWM scheme is employed for generating proper switching signals as shown in Fig. 3.



(a)



(b)

Fig.3 (a) Carrier-based PWM scheme for the generation of gating pulses (b) Control pulses

According to control scheme and gating signals as obtained above the switching signals of the power switches can be defined as,

$$T_c = \begin{cases} 1 & if \ v_{cona} > v_{t1} \\ 0 & if \ v_{t1} > v_{cona} > v_{t2} \\ -1 & if \ v_{t2} > v_{cona} \end{cases} \qquad (5)$$

Hence, switching functions can be written as

$$\left.\begin{aligned} S_{a1} &= \frac{T_c(T_c+1)}{2} \\ S'_{a1} &= 1 - S_{a1} \\ S'_{a2} &= \frac{T_c(T_c+1)}{2} \\ S_{a2} &= 1 - S'_{a2} \end{aligned}\right\} \qquad (6)$$

Therefore for phase 'A', in the positive half of the control signal v_{cona}, the switch S_{a2} is turned on and the line current is controlled by turning on or off the switch S_{a1}. In the negative half of v_{cona}, , S_{a1} is turned off and turning on or off S_{a2} can control the line current to follow the current command. For equal capacitor voltages ($v_{c1} = v_{c2} = v_0/2$), three voltage levels ($v_0/2$, 0, and $-v_0/2$) are generated on the AC side of the rectifier phase voltage v_{an}.

3. Results and Discussion

A simulation model of three-phase, neutral-point clamped, AC-DC, 3-level converter under balanced load is developed using SimPowerSystems in MATLAB/Simulink environment. Table 1 shows the simulation parameters for 6.6 kV system.

TABLE 1
Simulation Parameters

Phase Voltage (RMS)	V_{sa}	3810 V
AC Link Inductance	L_{ac}	30 mH
AC Link Resistance	R_{ac}	0.8 Ω
DC Link Voltage	V_{dc}	11000 V
DC Link Capacitance	C_1 and C_2	100000 µF each
Load Resistance (balanced load)	R_1	30 Ω
	R_2	30 Ω
Carrier Frequency	f_c	2 kHz

Fig.4 shows the phase voltage (V_{sa}) and line current (i_{sa}) at source terminals and it can be clearly seen that the converter is working at unity power factor for balanced load. Fig. 5 shows the harmonic spectrum of line current of phase 'A' which shows that harmonic content in the line current is well below the 5% limit. The voltage across the switch S_{a1} is shown in Fig. 6 which is only half of the total dc link voltage. The simulated waveforms for AC side line-to-line voltage (V_{ab}) and line-to-neutral voltage (V_{an}) of the converter are shown in Fig. 7 (a) and 7 (b).

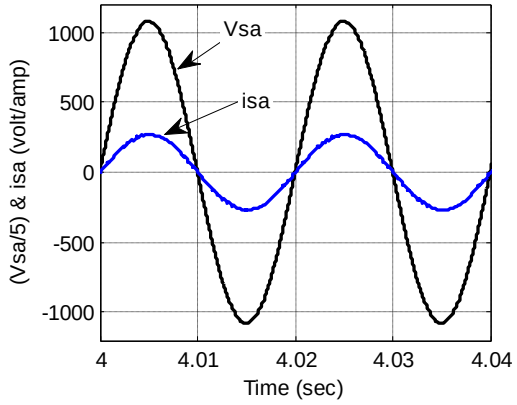


Fig. 4 Source phase voltage (V_{sa}) and line current (i_{sa}) under balanced load

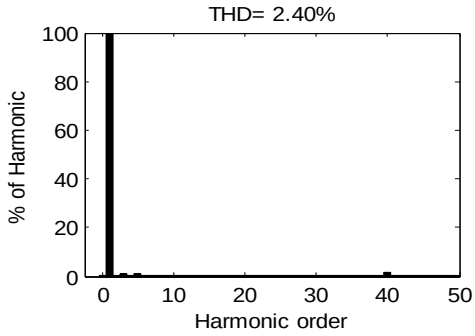


Fig. 5 Harmonic spectrum of line current (i_{sa}) under balanced load

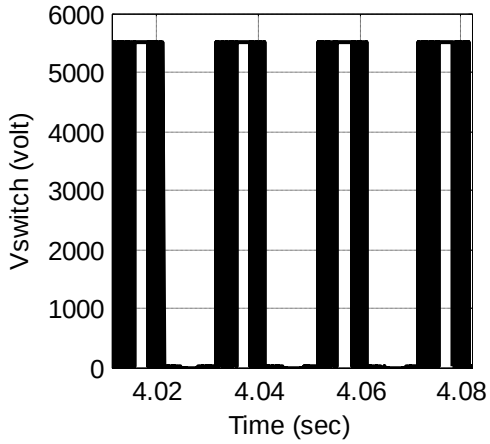
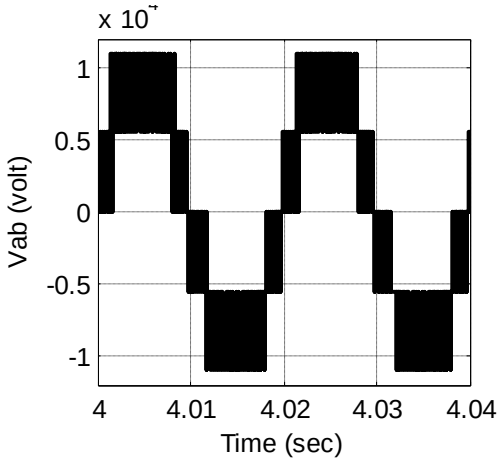
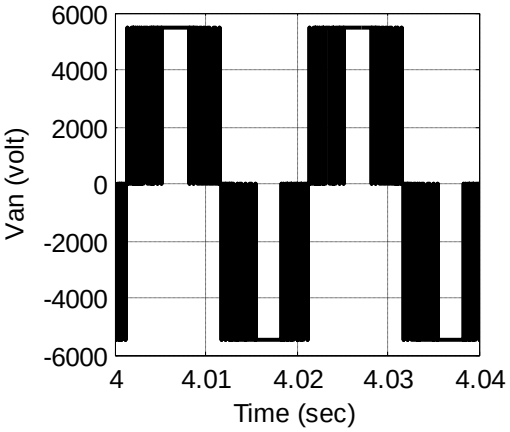


Fig. 6 Voltage across switch S_{a1} under balanced load



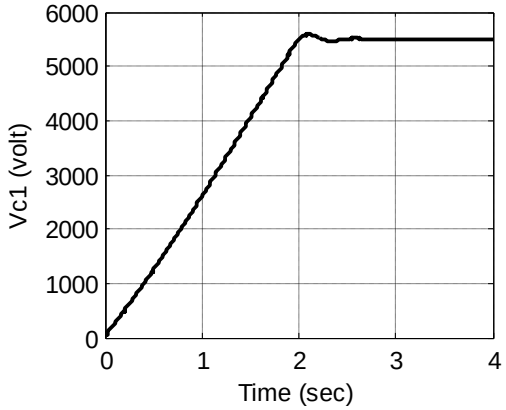
(a)



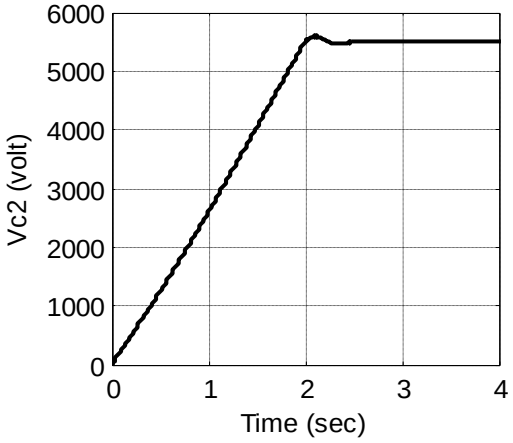
(b)

Fig. 7 (a) AC side line-to-line voltage (V_{ab}) (b) Line-to-neutral voltage (V_{an}) under balanced load

Under balanced loading condition, the voltages across the capacitors (C1 & C2) are shown in Fig. 8(a) & Fig. 8(b). From these figures, it can be observed that the voltages across the capacitors are almost balanced.



(a)



(b)

Fig. 8 (a) Voltage across dc link capacitor C_1 (b) Voltage across dc link capacitor C_2, under balanced load

4. Conclusion

The performance of a three-phase neutral-point clamped rectifier is evaluated for improved power quality and balancing of voltage across dc link capacitors, with simple control. Simulation results are presented to study the performance of the system under balanced load. The results shows that the proposed three-phase neutral-point clamped rectifier works at unity power factor and the THD of supply current is also well within the limits imposed by IEEE 519 standard under balanced load.

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