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Forward Body Biasing Technique in Current Folded CMOS LNA in Subthreshold Region for Biomedical Applications

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Abstract: A CMOS low noise amplifier with current folded technique has been proposed for ultra-low voltage, ultra-low power biomedical applications. The target frequency is 2.4 GHz and the proposed LNA is implemented in standard 65 and 90 nm CMOS technologies. By exploiting forward body biasing technique in current folded architecture, the LNA is biased in subthreshold region with supply voltage of 350 m V and DC current consumption of 503 uA. The LNA achieves power gain S21 of 10 dB, noise figure NF of 1.7 dB, IIP3 and P1dB of -8 dB, -18 dB respectively.

***Index Terms*— Ultra low voltage, forward body biasing, CMOS Low noise amplifier, 2.4 GHz, current folded technique, biomedical application, subthreshold region**

I. Introduction

THE Growing demand for implantable biomedical systems has motivated the development of low cost, low weight and highly integrated radio frequency transceiver used in wireless system networks for medical and health care application such as remotely controlling of drug delivery of patients or monitoring of patient's physiological parameters [1]. Recently, even more biomedical systems have been evolving due to advancement in circuit and scaling technologies. To name a few, pacemakers, implantable cardioverter defibrillators, neurostimulator, cochlea implants, drug infusion, implanted diabetes monitor are among most important ones.

Before implementation of these medical devices in RF communication, designers employed inductive link of 125Hz with very limited range. Therefore, to overcome this range limitation in outdated inductive medical systems, research was developed to enable operation in ultra-low power ultra-low voltage radio frequency integrated circuits in conventional CMOS technologies. The evolution of CMOS and its improved performances at high frequency would make it a lot easier to implement RF IC front-end with digital signal processor back-end on single chip integration. Advanced scaling in CMOS has been proven for many years to have better cut-off frequencies and noise performances. As shown in Fig. 1, new generation of wireless medical systems with

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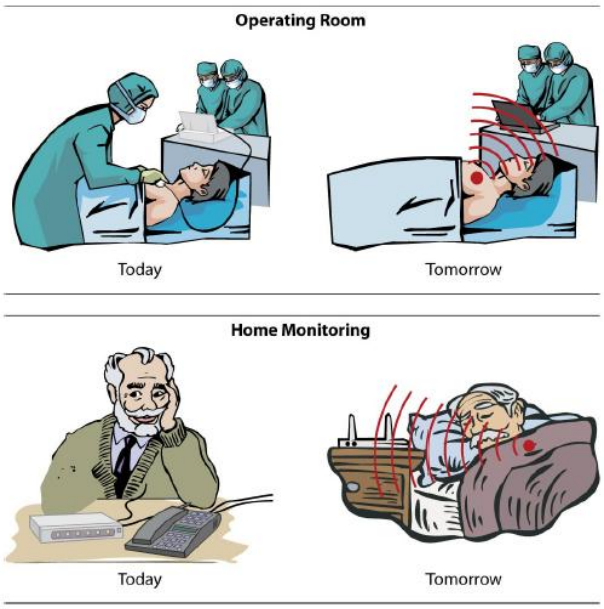

Figure 1. New medical implant devices with use of RF communication in integrated circuit technologies [2].

improved performance and eventually lower cost are being used lately by implanted medical device manufacturer such as Medtronic [2].

The design of transceivers in such medical devices is very challenging. Since most of these electronic biomedical systems operate with battery, for longer operation low supply voltage and low power transceiver is needed. The work in this paper presents low power, low noise amplifier (LNA) used in RF front-end transceiver with advanced techniques for low voltage operation [3-7].

Fig. 2 shows a simplified block diagram of a typical receiver. As it can be seen from the graph, the first active device after antenna is low noise amplifier. Note that the LNA has strong impact on input sensitivity of conventional receiver

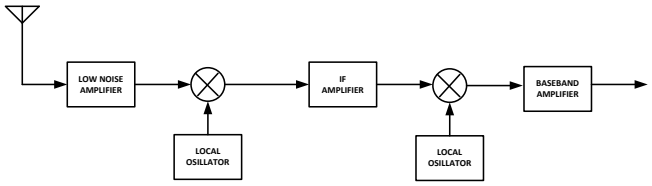

Figure 2. LNA as the first active stage in typical front-end receiver is shown.

frontend. Therefore, there is trade-off between gain and noise figure in selecting the architecture of LNA stage. The main function of LNA is to provide enough gain to overcome noise o later stage such as mixer. In addition, LNA is usually required to present specific impedance such as 50 ohm, add little noise and accommodate large signal without distortion.

Consequently, as the one of the most important building block of receiver and due to its continuous operation, it is very desirable to reduce supply voltage and total power consumption. It has remained as great challenge to design low power LNA at radio frequencies of multi-giga hertz due to non-idealities which appear at low power and low voltage operation. As examples, CMOS transistors appear to have lower gain due to reduction in transconductance and high noise figure when the power supply is scaled. The LNA is traditionally being implemented in an inductively source degenerated architecture as shown in Fig. 3 [3-7]. Furthermore, lower intrinsic gain of transistor at multi giga-hertz frequency will make it hard to obtain good noise performance and low noise figure (NF). Moreover, noise sources like gate-induce noise become more noticeable as the frequency of operation increases. In addition, it is usually biased in strong inversion region. This cascode topology requires two stack transistors it is not optimum solution for low voltage operation needed for biomedical electronic application [8-11].

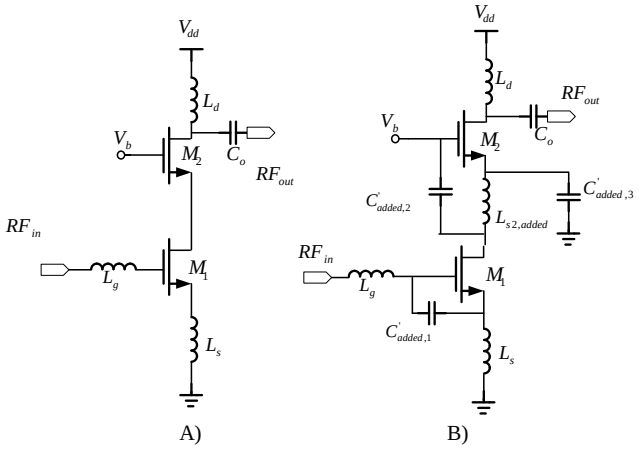

Figure 3. A) Conventional cascode inductive source degeneration LNA B) Current-reused CMOS low noise amplifier.

To overcome these limitations in this work, a low noise amplifier is implemented in folded current architecture with advanced forward biasing techniques. The conventional current folded low noise amplifier is shown in Fig. 3. As it can be seen from the figure, the two stack transistors are avoided and current is folded from NMOS transistor to PMOS transistors. Having one transistor between power supply and ground rail this topology, therefore, and as discussed more in detail later, is suitable for low voltage and low power applications. Furthermore, forward biasing technique as it will be shown in this paper is employed to scale the supply voltage. The CMOS transistors are biased in subthreshold region and hence it significantly reduces total power consumption. To simplify design the biasing networks which are implemented by two separate current mirrors are not shown in Fig. 2. With these considerations and proper design parameters, the satisfactory results were achieved which is explained in subsequent sections accordingly.

This paper organized as follows: section II introduce CMOS folded low noise amplifier and its potential for low voltage operation is described. The advanced forward biasing technique is discussed in detail. Circuit design parameters and the implementation of proposed work are addressed in section III. Simulation results are presented in section IV and comparison with recently publish LNA has been offered. Finally the paper is concluded in section V.

II. CURRENT FOLDED LOW NOISE AMPLIFIER

A. *Conventional and modified topology*

Designing LNA at giga frequency with low supply voltage and acceptable performances has lots of challenge as it was stated in introduction section. Conventional inductively source degenerated is popular architecture for low noise amplifier because of its advantages in terms of gain, noise figure, input matching and stability and it has been implemented in a couple of papers [9-11]. Note that the denegation improves also the linearity by forming a negative series-series feedback. However, it requires two stack transistors which results in higher supply voltages to bias the transistors and the performances worsen considerably as the voltage scaled and thus is not optimum for battery powered application which have low budget of voltage. On the other hand, the current folded architecture employs one transistor between power supply and ground rail which make it suitable for low voltage application. As shown in Fig. 4, in folded current LNA, RF signal amplified by common source NMOS transistor *M1* while common gate PMOS transistor *M2* with unity gain act as buffer to separate input and output tanks and ease stability issues at high frequencies [12,13]. In the Fig. 5 the modification of conventional current folded is proposed with adding the two capacitor which otherwise would make design more complicated. The advantages of these would become apparent shortly as they avoid the very large inductors. In some cases these inductors are too big to implement on-chip

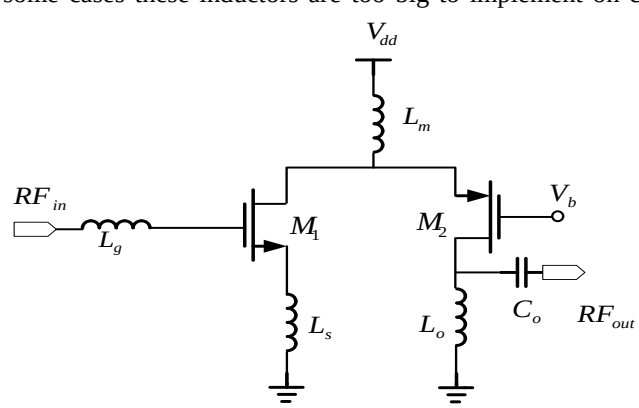

Figure 4. Conventional current-folded CMOS low noise amplifier.

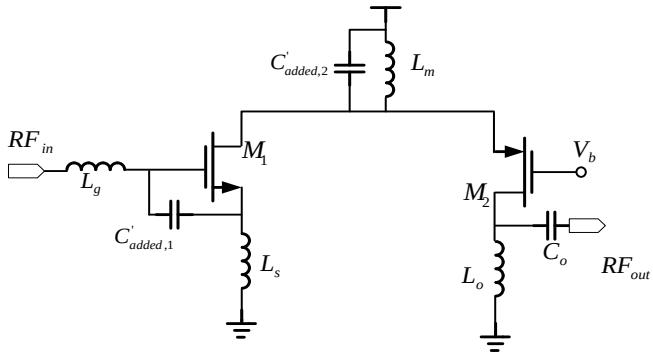

Figure 5. Modification of current-folded CMOS low noise amplifier with adding capacitances.

and some designers used off-chip inductors to implement the circuit [12]. It is another advantage of this work that all components are fully integrated.

B. Input matching

Similar to conventional cascade architecture, source Inductor L_s resonate with gate to source capacitance C_{gs} and with remaining parasitic capacitance set input matching to the signal source of 50 ohm impedance at desired frequency. Note that gate inductor L_g is employed to facilitate impedance matching avoiding large value of source inductor. In addition, $C_{added,1}'$ is added to compensate small value of C_{gs} at low supply voltage and small ratio of transistors. Therefore, this capacitance with internal gate to source and parasitic capacitance of transistors will tune with total gate and source inductances at desired frequency of 2.4 GHz. The inductors and transistor parasitic resistances also have contributions to total input impedance. With respect to this the input impedance formula can be approximated by [14]:

$$Z_{in} = r_g + r_s + r_{Lg} + r_{Ls} + \frac{g_{m1} L_s}{(C_{gs1} + C_{added,1}')} + j\left(\omega_0(L_g + L_s) - \frac{1}{\omega_0(C_{gs1} + C_{added,1}')}\right) \quad (1)$$

where r_{Lg}, r_{Ls} represents parasitic resistance of the inductors, r_g and r_s stand for gate and source parasitic resistances, C_{gs} represents for parasitic gate to source capacitance, $C_{added,1}'$ is the added capacitor, ω_0 is resonant frequency, g_{m1} is small signal transconductance of NMOS transistor M_1. According to this observation the input matching to source impedance of 50 ohm is obtained by the purely resistive of real part of equation (1). It should be noted that even this formula cannot be used to predict the exact value for input matching and computer simulation is most of the time necessary for more accurate results. However, it will be helpful to have more insight for design implementation stage.

Inductor L_m act as a low resistance for dc bias current of both transistors and with parasitic capacitance of the node is tuned at center frequency ω_0 to prevent losing of RF signal to power supply. In the same justification as before for $C_{added,1}'$, the capacitance $C'_{added,2}$ was added to avoid large value of inductor L_m and tune the tank circuit. In fact, this simple modification greatly helps in design implementation since relaying on only parasitic capacitance would leads to employing much bigger inductor while with proper selection of adding $C'_{added,2}$ this issue can be mitigated. The tank shows high impedance at the center frequency ω_0 which make the RF current to be folded into source terminal of PMOS transistor M_2. It is also the reason that this architecture has been named as current folded topologies. However, this architecture can be further modified for low voltage application by scaling threshold voltage and therefor supply voltages by forward body biasing technique as it will be discussed shortly.

C. CMOS forward biasing in current folded

Forward body biasing technique with triple-well complementary metal oxide semiconductor technology and also its proposed implementation in current folded low noise amplifier has been shown in Fig. 6 and Fig. 7, respectively. The reasons for using forward biasing technique is that one of the main consideration of CMOS technology and its application for low voltage operation is the threshold voltage of NMOS transistor. It is beneficial to have low threshold voltage transistors so that supply voltage can be scaled accordingly. For the conventional CMOS technology the transistor with multiple threshold voltage has been implemented by changing the thickness of the multiple gate oxide and channel doping. But this solution, will leads to higher cost of fabrication and it will complicate manufacturing process.

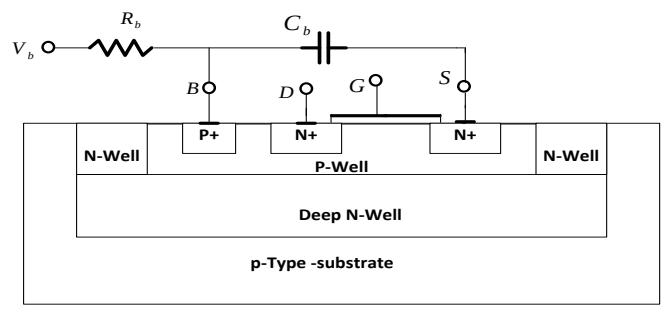

Figure 6. The proposed forward body biasing technique. This is applied to the modified current-folded CMOS low noise amplifier in this work.

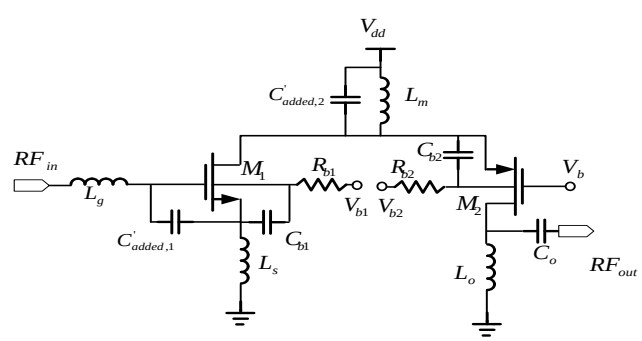

Figure 7. The proposed architecture with forward body biasing technique applied to the modified current-folded CMOS low noise amplifier.

As a result, it is appropriate to adjust the transistor threshold voltage by circuit implementation without adding extra steps in fabrication and the cost associated by it. The NMOS transistor threshold voltage can be approximate by [13]:

$$V_{th} = V_{th0} + \gamma\left(\sqrt{|2\varphi_F| + V_{SB}}\right) - \left(\sqrt{|2\varphi_F|}\right) \quad (2)$$

where V_{th0} is threshold voltage for source-to-body V_{sb}=0, γ process-dependent parameter and φ_F semiconductor parameter and its value is around 0.3 to 0.4V.

Thus, the bias voltage at body terminal can be adjusted to change threshold voltage of CMOS transistor. Forward body biasing V_b will decreases threshold voltage of transistor and therefore makes transistors able to operate in lower supply voltage. Forward body biasing technique in cross sectional of NMOS for typical triple-well CMOS process shown in Fig. 5, increases body voltage and will make source to body voltage V_{sb} negative and consequently threshold voltage V_{th} reduces. Another important consequence of this reduction of transistor threshold voltage is that the transconductance maintained high at low voltage which effectively increased gain of the LNA.

As it was shown in Fig. 6, note that resistor R_{b1} and R_{b2} limit the overhead dc bias current due to forward body biasing and this resistors prevent latch-up effect in CMOS. Body capacitance C_b avoids the reverse impact on the body transconductance g_{mb} in terms of RF gain. It can be further understood by noting that the body transconductance g_{mb} is in opposite direction with transconductance g_m and capacitance C_b eliminates negative effects of it on small signal RF gain. Therefore the capacitance C_b can be viewed as a gain enhancement parameter.

It should be also noted that forward body biasing in fact add one more design parameter which will leads to have more flexibility and freedom in design implementation. The values of design parameters can be obtained intuitively and by experiences and the more accurate design parameters and results can be optimized by computer simulation as it will be discussed in section *III*.

For biasing of the LNA to separate current mirror were implemented to control the dc current of transistor efficiently and make them to operate in subthreshold region to reduce power consumption.

D. Noise Factor

One measurement of a system is the noise performance that usually defined as noise factor, F, as follows [16]:

$$F = \frac{\text{total output noise power}}{\text{output noise due to input source}} \quad (3)$$

where the source noise is at a temperature of 290K. In the other words, noise factor is simply the noise degradation of a system and the larger value means larger degradation. In an ideal case, if the system doesn't add any noise by itself and therefore output noise is entirely due to source, the noise factor will be equal to unity.

Noise Factor (F) in nanometer CMOS technology can be given approximately as [14]:

$$F = 1 + \frac{1}{R_{source}}\{R_g + R_{Lg} + R_s + R_{Ls} + |Z_T|^2 \frac{\overline{|i_g^2|}}{4KT\Delta f} + \left|\frac{1 + j\omega C_{gs} Z_t}{g_m}\right|^2 \frac{\overline{|i_d^2|}}{4KT\Delta f} - 2Re[Z_t\left(\frac{1 + j\omega C_{gs} Z_t}{g_m}\right) * \frac{\overline{|i_g^2 * i_d^2|}}{4KT\Delta f} \quad (4)$$

Where Z_s impedance of signal source, K is the Boltzmann constant, T is absolute temperature, i_g is induced gate noise current, i_d is the drain noise current, R_{source} is the signal source resistance of 50 ohm, R_g and R_s account for parasitic gate and source of transistor, R_{lg} and R_{ls} parasitic resistance associated with gate and source inductors respectively, and $Z_t = Z_s + R_g + R_f + R_{Lg} + R_{Ls} + j\omega (L_g + L_s)$.

E. Linearity

The linearity of LNA needs to be considered in advanced transceiver systems. In homodyne receiver, even-order harmonics create DC offset whereas subsequent of mixing with interfere in adjacent channel, third-order intermodulation distortion corrupt the desired down-converted signal. It should be noted that adding the input capacitor $C'_{added,1}$ improves the linearity of the LNA. According to a simple nonlinear polynomial model of MOSFET, IP3 can be improved by increasing the effective $C_{gs.}$ [15]. Furthermore this results, was suggested to be hold for different transistor sizing and biasing current. Therefore, adding the parallel C_{gs}' in fact will mitigate the use of relatively small transistor in this design. This would alleviate the pretty poor performance in terms of linearity of low noise amplifier at low supply voltages. Another important consideration is that according to rule of thumb in RF and general formula for input-referred third-order intercept point later stage has more impact on linearity. General formula can be approximated by [l6]:

$$\frac{1}{IIP3,total} \approx \frac{1}{IIP3,A} + \frac{G_A}{IIP3,B} + \frac{G_A G_B}{IIP3,C} + \cdots \quad (5)$$

where the *IIP3,A* represent the input-referred third-order intercept point of first stage which is the LNA and G_A represents its gain. In the same manner, B and C represent the corresponding next staged which are usually mixers. It should be pointed out the linearity trades of with gain in above equation. Later active stages in receiver chain such as mixer play more important role in total linearity of whole system. Section *IV* will evaluate the third-order behavior of the proposed CMOS LNA for RF application.

F. Subthreshold conditions

Using two separate current mirrors for NMOS and PMOS transistor biasing, facilitate design further. The two transistors were biased accordingly in subthreshold region. Note that

MOSFET subthreshold region has been implemented widely for ultra-low power analog circuits where it has been presented that in weak inversion the key benefit is associated with higher ratio of transconductance to dc bias current compared to strong region ratio [17]. It is already shown also that digital CMOS for ultra-low power applications can be implemented in weak inversion where power supply voltage is usually less than transistor threshold voltage. Weak inversion in fact, will require less voltage headroom which results in further reducing supply voltage [17].

Although the ratio of transconductance to dc bias current is relatively higher in subthreshold region, still the transconductance itself is lower than strong inversion region. Therefore, as it is implemented in this work, transistor with pretty large device ratio is used to compensate the low transconductance in weak inversion and achieve value comparable to strong inversion with much lower bias current. This technique as a matter of fact is enormously helpful and leads to tremendously low power consumption.

G. Cut-off frequency of CMOS

High frequency of merit f_t has been defined at which the current gain extrapolated to fall to unity. Assuming gate to source capacitance dominating the input capacitance and ignoring short channel effects on charge sharing, the simplified cut-off frequency in strong region can be approximate by [l6]:

$$f_t \approx \frac{g_m}{2\pi C_{gs}} \approx \frac{1}{2\pi}\frac{(\mu_n C_{ox}/2)WE_{sat}}{\frac{2}{3}WL\,C_{ox}} \approx \frac{1}{2\pi}\frac{3\mu_n E_{sat}}{4\,L} \qquad (6)$$

Where $\mu_n$mobility of electron, *Esat* is the field strength at which carrier velocity has dropped to half of value extrapolated from low-field mobility. As it can be inferred from this equation, the cut-off frequency of CMOS transistor in short channel device is proportional to 1/L rather than $1/L^2$. Also in strong region it is not depends on bias conditions. With shrinking the length of MOSFET transistor, f_t of more than 150 GHz is common case. It is also another reason CMOS devices are increasingly implemented in application than previously were found in bipolar or GaAs technologies.

On the other hand, the cut-off frequency of transistor is lower in subthreshold region compare to strong region and can be approximated by:

$$f_t = \frac{1}{2\pi} + \frac{I_D}{\left(\frac{KT}{q}\right)}\frac{1}{WLC_{js}} \qquad (7)$$

Where I_D is dc bias current and C_{js} is depletion region capacitance. However, as it can be seen from above formula, the scaling technology improved the cut-off frequency even in subthreshold region to higher values such that it would be in acceptable range for applications with multi-giga hertz frequencies. With respect to equation (7) it is clear that implementing the circuit with minimum length again here will make the better performance in terms of cut-frequency as it exploited in this work.

III. Design implementations

The objective of this design is to implement a low cost low noise amplifier with low supply voltage suitable for biomedical application while maintain low noise figure. With iteratively simulation and proper design parameters for each component, optimum performance was achieved. The summery of design parameter is shown in table 1. By forward body biasing technique and supply voltage scaling down to 350 mV, transconductance gm_1, gm_2 of 23 mS and 21 mS were achieved.

For transistor sizing, minimum length 90 nm was chosen with optimized widths of 50 um and 400 um for NMOS transistor M_1, and PMOS transistor M_2, respectively. Thus, the proposed circuit simultaneously achieves high transconductance and low dc bias current of total 502 uA. The current limiting resistance R_{b1}, R_{b2} of 1 k-ohm, and enhanced gain capacitors C_{b1} and C_{b2} of 2 pF was chosen by effective circuit simulations.

The inductors values for L_g, L_o, L_m, L_s are optimized at 8.5 nH, 5 nH, 6 nH, 800 pH respectively to tune the proposed low noise amplifier frequency of interest at 2.4 GHz with associated capacitances. The capacitance values for $C'_{added,1}$, C_o and $C'_{added,2}$ of 500 fF, 100 pF, 500 pF were chosen accordingly. With respect to these considerations and based on folded current topology ultra-low voltage ultra-low power was implemented. Simulation results

The power gain S21 and input matching S11 are plotted versus frequency in Figure. 7. As it can be seen from the graph the proposed low noise amplifier achieves 10 dB power gain at 2.4 GHz with power supply V*dd* of only 350 mV and DC current of 502 uA. These incredible results were due to forward biasing and proper choices of parameter values for current folded topology. The gain is determined by NMOS transistor M_1 and can be increased by altering the biasing current through it. Beside intuitive approached, extensive iterative simulation is usually needed to acquire the optimum performance. Input matching S11 of -20 dB is also shown in this graph.

As it was explained in section II, the CMOS device operating near subthreshold instead of saturation region will reduce total power consumptions. Therefore, noise modeling at high frequency in CMOS transistor operating in weak inversion has been recently analyzed and modeled in various papers where systematic of noise model has been shown [11]. Having noise factor introduce in section *III-C*, noise figure NF is simply noise factor expressed in decibels. Simplified minimum noise figure in subthreshold region in nanometer range technology presented in [11]:

$$NF_{min} = 1 + k\frac{2\pi f C_{ox} WL}{\sqrt{g_m}}\sqrt{r_g + r_s} \qquad (8)$$

where K is fitting constant, C_{ox} is the oxide capacitance per unit area, g_m is transconductance of transistor., respectively. As it can be inferred from the above formula, lower transconductance (g_m) is compensated with lower gate resistance r_g in subthreshold region to keep the noise figure in satisfactory range.

TABLE I. COMPONANT VALUES

Components	Values
W1(um)/ L1(nm)	50/100
Lg(nH)	8.5
Ls(pH)	800
W2(um)/L2(nm)	400/100
Vb2(mV)	450
Vb1(mV)	400
Cb1, Cb2(pF)	2
Rb1, Rb2 (K)	10
Lm(nH)	6
C,'added1(fF)	500
C,'added2(pF)	500
Lo(nF)	5
Co(pF)	100
Id(uA)	502
Vdd(mV)	350

Noise figure NF and minimum noise figure NF,$_{min}$ as a function of frequency is plotted in Fig. 8. The value of 1.7 dB and 1.1 dB were achieved for NF and NF,$_{min}$ at frequency of interest. Thus, this design can be a possible candidate for relatively low noise application as well.

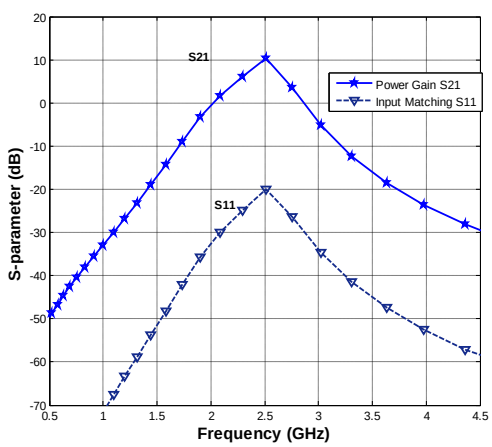

Fig. 8. Power gain (S21) and input matching (S11) versus operating frequency of proposed low noise amplifier at 502 uA DC current.

Input-referred third-order intercept point (IIP_3) for the proposed low noise amplifier. In Fig. 9 input-referred 1dB comparison point P1dB of the current folded LNA is shown versus frequency. The value of -18 dBm is obtained. In Fig. 10 input-referred third-order intercept point (IIP3) for the proposed low noise amplifier at 350 mV supply voltage is plotted versus frequency and it achieves – 8 dBm.

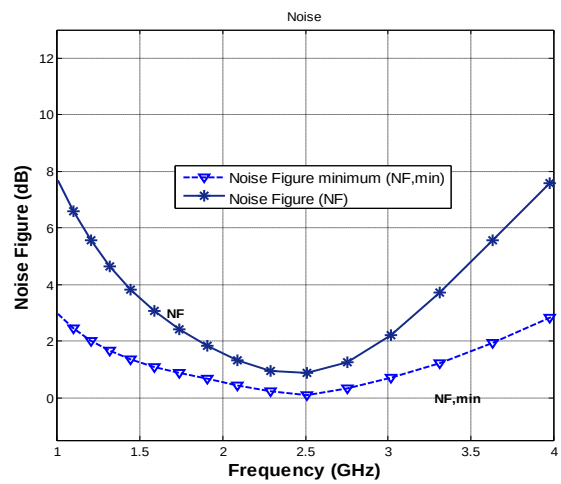

Fig.9. Noise figure (NF) and minimum noise figure (NFmin) of the proposed LNA versus operating frequency at 502 uA DC current.

Input-referred third-order intercept point (IIP_3) for the proposed low noise ampilifier. In Fig. 9 input-referred 1dB comparison point P1dB of the current folded LNA is shown versus frequency. The value of -18 dBm is obtained. In Fig. 10 input-referred third-order intercept point (IIP3) for the proposed low noise amplifier at 350 mV supply voltage is plotted versus frequency and it achieves – 8 dBm.

Having several performance aspects, the figures of merits (FOMs) have been proposed [10] to characterize overall performance of low noise amplifier:

$$FoM1 = \frac{S_{21}\,[dB]}{P_d\,[mW]} \qquad (9)$$

$$FoM2 = \frac{S_{21}\,[dB]}{(NF[dB]-1)\,.\,P_d\,[mW]} \qquad (10)$$

$$FoM3 = \frac{S_{21}\,[dB]\,.\,IIP3[mW]\,.f\,[GHz]}{(NF[dB]-1)\,.\,P_d\,[mW]} \qquad (11)$$

With higher value representing better performance, as it is shown in Table II, due to advantages of forward biasing technique in current folded architecture with employing proper design parameters, the LNA in this work achieves superior overall performance compared to state of art LNAs which have been published recently. Note among to have a fair and better comparisons similar works where considered.

TABLE II. SUMMERY OF COMPARISON BETWEEN THE STATE OF ART LOW NOISE AMPILFIER AND THE PROPOSED CURRENT FOLDED LNA IN 90 NM CMOS

	This work	[18]	[19]		[20]	[21]	[22]
F (GHz)	2.4	2.4	2.4		2.4	2.4	2.4
Gain S21 (dB)	10	13	16.42	17.27	22.7	16.5	14.3
NF (dB)	1.7	4.9	1.88	1.9	2.8	0.78	3.1
S11(dB)	-20	-18	-45	-54	-14.7	-19	-15.4
Vdd(V)	350	0.5	0.6	0.6	1	0.5	1
Idd(mA)	0.502	5.6	2.49	3	-	-	-
Pd(mW)	0.176	2.8	1.45	1.80	0.943	3.3	16
P1(dB)	-18	-18	-29	-29	-10	-20.9	-
IIP3(dBm)	-9.5	- 9	-15	-13.3	5.14	-	-11.6
FoM1(dB/mW)	56	4.64	11.3	9.56	24	5	0.9
FoM2(1/mW)	100>	1.19	10.36	10..06	13.37	22.3	0.425
FoM3(GHz)	24	0.015	0.02	0.02	3.2	-	0.07
Technology(CMOS)	90 nm	90 nm	90 nm		90 nm	130 nm	90 nm

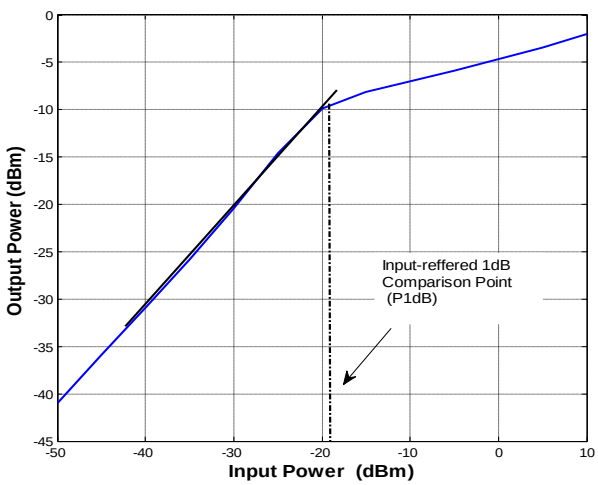

Figure 9. Input-referred 1-dB compression point for the proposed current folded LNA.

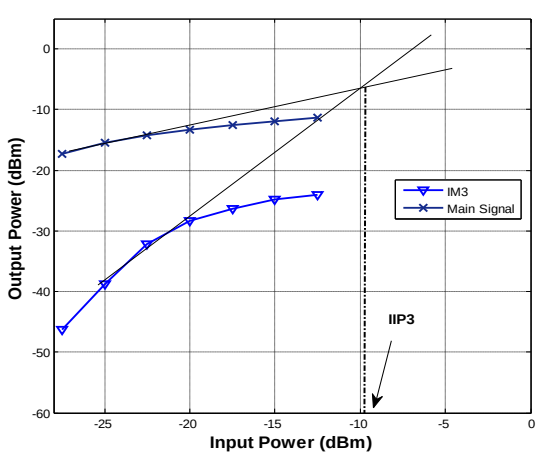

Fig .11.Input-referred third-order intercept point (IIP_3) for the proposed low noise ampilifier.

IV. Conclusion

An ultra-low voltage low power LNA with current folded architecture was implemented in 65 nm and 90 nm CMOS digital technology target ISM band frequency for biomedical application. To have a better comparisons with other related and similar works, values presented here are on 90 nm technologies. The circuit technique of forward body biasing was exploited to reduce supply voltage down to 350 mV while maintain the satisfactory performance results. The LNA achieves power gain of 10 dB, low noise figure of 1.7 dB and high linearity input refer third order IIP3 of -8 dBm with dc current of 503 uA while consume remarkably only 176 uW.

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