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Effects of Metal Gate Electrode and HfO_2 in Junction less Vertical Double Gate MOSFET

Jagdeep Rahul, Shekhar Yadav, Vijay Kumar Bohat
VLSI Design Lab, Lovely Professional University, Phagwara ,Punjab, ABV-Indian Institute of Information Technology and Management , Gwalior, M.P., India
Email: jagdeeprahul11@gmail.com

Abstract
- In this paper, we propose a novel design analysis for a Junctionless Double Gate Vertical MOSFET (JLVMOS) with metal gate electrode and HfO_2, for which the simulations have been performed using TCAD (ATLAS), The simulated results exhibits significant improvements in comparison to conventional JLVMOS device with a polysilicon gate electrode and ITRS values for different node technology . In place of polysilicon gate and SiO_2 we have used metal gate and hafnium dioxide (HfO_2) respectively and observed that metal gate electrode with HfO_2 in JLVMOS shows drain current is 1.77 mA, for a gate voltage of 1V and an average subthreshold swing, DIBL (Drain Induced Barrier Lowering) effect and leakage current are 61.01mV per decade, 40.4mV/V and 1.4nA/μm respectively. This significant improvement in drain current can be exploited for various low power high-performance circuit applications.

Keywords*:*
DIBL, Junctionless Vertical Double Gate MOSFET (JLVMOS), DIBL (Drain Induced Barrier Lowering), leakage current (I_{OFF}), Subthreshold Swing (S. Swing), TCAD Tool.

I. INTRODUCTION

The scaling of CMOS technology in to nano-meter regime requires alternative device structures in overcoming a number of short channel effects and leakage current. The formation of PN junction between the source/drain and channel become a fabrication challenge beyond 32 nm CMOS technology. A lot of novel double gate MOSFET structures have been proposed and widely investigated by number of researchers [1]. The Junctionless double gate vertical MOSFET has been proposed recently. The Junctionless VMOS is free from variety of challenges related to formation of source –drain junction with substrate and hence present a very suitable candidate for future deca nanometer MOSFET applications. In Junctionless VMOS, the doping level in the semiconductor source, drain and substrate is identical (n-type: N^+ - N^+- N^+ and p-type: P^+- P^+- P^+) and there is no formation of P-N junction between the source – drain and channel [2]-[3]. Gate is highly doped with p-type impurity (boron) to maintain the threshold voltage.

The advantages of vertical MOSFET is that it does not require next generation or advanced lithography to achieve a small memory area or a short channel length because it's defined by the sub lithography of layer thickness and etching [9]. The requirement of memory and logic application is different; on the one hand, memory cell area should be small for higher density so It can be achieved by using vertical MOSFET with small foot print but long channel length to reduce the OFF state current of circuit but the channel length for high performance logic should be short as much as possible for high ON state current. In Junctionless VMOS, the controlling capability of gate over the channel region, resulting in reduced short-channel effects (SCEs) [4]. The fabrication process of Junctionless MOSFET is highly simplified, in comparison to conventional CMOS technology. Since there are no doping concentration gradients required during the time of fabrication in the device, it also saves a lot of thermal budget[9]. The vertical channel of a VMOS is defined by gate spacer due to which the fabrication cost can be decreased drastically [5].

Now days industry's demands more integrated circuit functionality and higher performance at lower cost requires higher packaging density of transistors. The scaling of transistor size has force to reduce the channel length and gate dielectric thickness as well as supply voltage to maintain the constant electric field inside the channel. The silicon dioxide (SiO_2) thickness can be reduced up to 1.3 nm but there are several device parameter must be balanced during this process.

Many high-k materials have potential to replace the SiO_2 in future technology as a gate dielectric material below 2nm oxide thickness. The selection of high-k materials depends on the several properties like permittivity, band gap, and interface quality with silicon, thermodynamic stability and compatibility with current fabrication process of CMOS technology. Many dielectric materials have some property but very few materials are good with respect to all these properties. The Selection of gate dielectric with higher permittivity than that of SiO_2 is essential. The interface property of gate dielectric oxide with silicon substrate and gate electrode is very important in regards to device performance.

In this paper, the metal gate of a tunable work function (Φ_M) ranging from 5.0eV to 4.8eV has been used with hafnium dioxide (HfO_2) and investigated in JLVMOS for performance enhancement by using our two dimensional ATLAS simulator.

II. Device Structure And Simulation

The TCAD Tool package (DEVEDIT) is used to design the device structures and perform the relevant device simulations using ALTAS 2D simulator. The structure of JLVMOS with the double gate region (in contact), drain and source electrode, channel length (L_g), oxide thickness (T_{ox}), body thickness(T_{si})

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or channel and the respective dimensions of the device are explicitly shown in fig.1.The carrier depletion effect in the MOSFET due to the polysilicon gate electrode is also called as the poly depletion effect. It occurs when an applied electric field sweeps away carriers so as to create a region in the doped polysilicon where the non-mobile dopant atom becomes ionized. In p-doped polysilicon the depletion layer includes ionized non- mobile acceptor sites. This poly depletion effect reduces the strength of the expected electric field at the surface of the semiconductor when a voltage is applied to the gate electrode. The reduced electric field strength degrades the performance of the device. Metal gate electrode removes the carrier depletion effect observed in polysilicon gate electrode. It improves the device performance, at the same time, by maintaining the work function (Φ_M) equal or at least near to the value of polysilicon gates. The threshold voltage of JLVMOS is depends on the work function (Φ_{MS}) difference between the semiconductor and the material using at gate electrode. The metal gate electrode with work function near to 5.27 eV can replace the p- doped polysilicon typically found in N-type junctionless MOSFET.

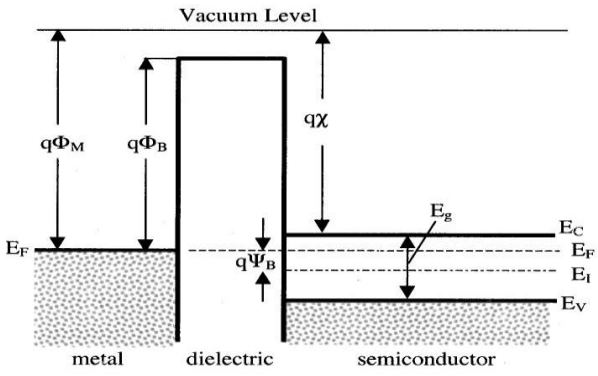

Fig.1: Energy-band diagrams of JLVMOS with metal gate electrode.

Where ϕ_m is the work function of metal gate electrode, χ is the electron affinity of semiconductor, E_g is the semiconductor band gap of n-type substrate, ϕ_B is the potential barrier between the metal gate and gate dielectric, and ψ_B is the potential difference between the Fermi level E_F and the intrinsic Fermi level E_I .

The gate oxide material with a dielectric constant (k) substantially higher than that of SiO_2 (k_{ox}), which will achieve a smaller Equivalent oxide thickness (EOT) than the SiO_2, even with a physical thickness ($t_{physical}$) larger than the SiO_2(T_{ox}):

$$EOT = \frac{k_{ox}}{k} \times t_{Physical}$$

The Replacing of SiO_2 with a high-k material having a different dielectric constant is not as simple as it may seem. The material bulk and interface properties of high-k materials should be good as compare to SiO_2 [10]. Basic properties of material like thermodynamic stability with respect to silicon, stability under thermal conditions relevant to nano-electronics fabrication, low diffusion coefficients and thermal expansion are some critical examples. Charge trapping and reliability for the gate dielectrics are particularly important considerations. The dielectric constant of HfO_2 is approximately 25 has been used with metal gate electrode in Junctionless Vertical Double Gate MOSFET. The high-k material hafnium dioxide (HfO_2) with physical thickness of 3nm is used in the place of silicon dioxide but the EOT is about 0.5nm which improves the controlling capability of gate over channel.

We assumed high channel doping concentration ($1\times10e\text{-}^{19}cm\text{-}^{3}$) for less V_t variations. Silicon film thickness and oxide (HfO_2) thickness are 10 nm and 3nm, respectively. We assumed N-channel device for different work function of metal gates of JLVMOS. A good match of work function can be obtained by using nickel (Ni) and gold (Au) for gate electrodes of JLVMOS. The work function of p-doped polysilicon is found approximately 5.27 eV. We assumed that nickel metal for metal gates because it provides wide range of work function. Metal gate technology may potentially replace conventional polysilicon gate technology for juctionless devices for better performance.

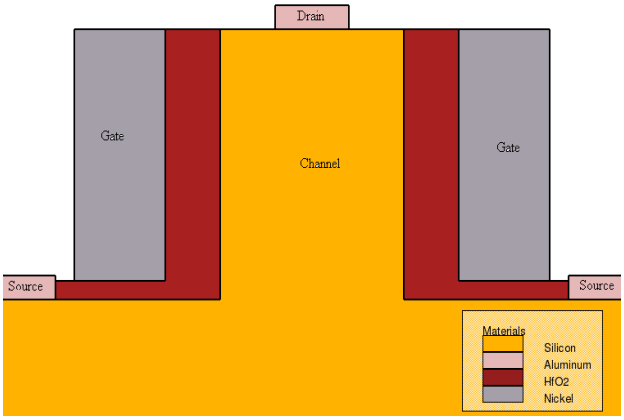

Fig.2: 2D Structure of Junctionless Vertical Double Gate MOSFET.

III. RESULTS AND DISCUSSION

The JLVMOS structure with high work function (WF= 5.0eV) using HfO2 as a gate dielectric has lower DIBL (drain induced barrier lowering), subthreshold swing, low leakage current and higher threshold voltage as compared to devices having gate electrode with work function (WF=4.80eV) but lower drain current shown in table 1. The JLVMOS having metal gate electrode with work function 4.8eV has higher value of Idmax (maximum drain current) compared to metal gate device with work function 5.0eV, 4.9eV with HfO_2 and polysilicon gate electrode with SiO_2, but it has higher leakage current, subthreshold swing and DIBL effect. So by providing the different work function of metal gates to JLVMOS device we can set the appropriate threshold voltage. So we are able to increase the drain current according to our requirements without adding any extra doping in to the channel because drain current is affected by work function of metal gate electrode. The short channel effects like DIBL and subthreshold swing of JLVMOS with HfO_2 and metal gate electrode with workfunction of 4.8eV are 40.4mV/V and 61.01mV/dec respectively due to better control over on channel region of the device. The use of HfO_2 in

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JLVMOS increases the interface charges density at the surface of HfO_2 and degrade the mobility due to which the gate capacitance get increased up to the 60%.Which degrades the device performance but at the same time the device with work function of 4.8eV has produced 1.77mA/µm of drain current and leakage current is less than 1.42nA/µm. These results are better than conventional JLVMOS with poly silicon gate electrode and SiO_2 as a gate oxide material.

The I_d-V_{gs} characteristics of Junctionless Vertical Double Gate MOSFET is shown in fig.3 and I_d-V_{ds} characteristics are shown in fig.4 drain current of JLVMOS with work function of 4.8 eV is 1.77mA, which is high comparison to the JLVMOS with polysilicon gate. The I_d-V_{ds} characteristics of JLVMOS has been obtained at gate voltage of 1.0 V and found that when we decreases the work function of gate electrode, the drain current of JLVMOS start to increase because the channel surface below the gate electrode start accumulating earlier and produce large drain current without adding any extra doping in the substrate. The Metal gate with high-k material (hafnium dioxide) in JLVMOS has produced better results in terms of drain current and leakage current and also it's highly immune to shorts channel effect like DIBL and subthreshold swing

Advantages of metal gate and high-k material over polysilicon gate are there is virtually no depletion, no boron penetration, and sheet resistance is very low.

Table1: Comparison table of JLVMOS with metal gate electrodes and HfO_2 at difference work function.

Device	Idmax (A/um)	Leakage Current(I_{OFF})	DIBL (mv/v)	S.Swing (mV/dec)
Poly Gate +SiO2	**7.2×10^{-4}**	**1.134×10^{-10}**	**44.29**	**63.74**
Metal gate (ϕ_m =5.0eV)	**0.001070**	**7.191×10^{-13}**	**35.6**	**60.55**
Metal gate (ϕ_m =4.9eV)	**0.001429**	**3.216×10^{-11}**	**38.2**	**60.7**
Metal gate (ϕ_m =4.8eV)	**0.001772**	**1.422×10^{-09}**	**40.4**	**61.01**

Table1 values are better than the ITRS values for 45nm node technology for both low power and high performance logic application. The drain current of device can be increased by using metal gate electrode with low work function in comparison to polysilicon gate electrode because channel is already highly doped if we will add any extra doping in to the channel it will degrade carrier mobility in high temperature environment.

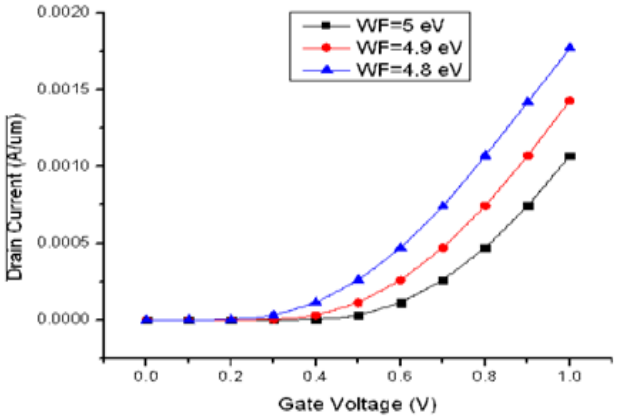

Fig. 2: I_d-V_{gs} Characteristics of JLVMOS at 45nm Technology.

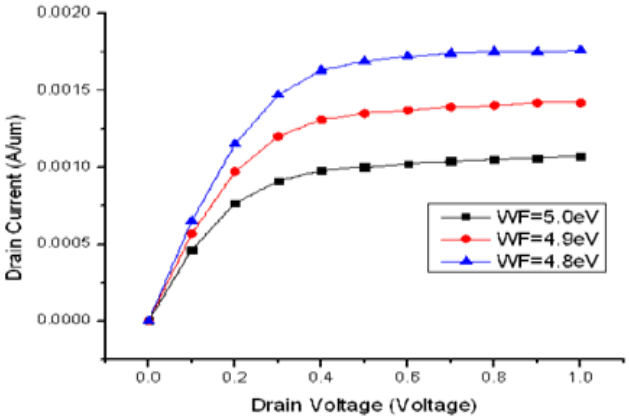

Fig.3: I_d-V_{ds} Characteristics of JLVMOS at different gate voltage of 45nm technology.

IV. CONCLUSION

The work function engineering is the concepts by which we can set the appropriate threshold voltage of JLVMOS device that provide better device performance compared to the channel doping. The metal gate electrode with high-k materials produced better device characteristics, high drain current and low leakage current with average subthreshold swing and DIBL effect. These results are significantly better than ITRS results for 45nm technology for both low power as well as high performance circuit applications. It also allows a thinner effective dielectric thickness without affecting device performance. The metal gate electrode in JLVMOS with work function 4.8eV produced highest drain current which is 150% more than the polysilicon gate electrode in same device and the DIBL effect, S. Swing and leakage current are still in the acceptable range. The capacitance of JLVMOS will get increased by 60% due to the high-k materials still the performance of JLVMOS will get improved by near about 70% in comparison to conventional JLVMOS. In comparison to SOI technology the use of bulk silicon as a starting material for fabrication of the JLVMOS has better capability for heat dissipation.

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