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Study and Implementation of Programmable DDC in SDRP

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Abstract— A Digital Down Converter (DDC) is an integral part of any Software Defined Radio (SDR) module. Digital down conversion causes a band limited high sample rate signal to be shifted to low frequency and also the sample rate of signal is reduced without losing information thereby simplifying further processing. A DDC design is efficiently implemented using programmable filters available in AD9361 transceiver together with an optional programmable design implemented on SOC.

Keywords— Digital down conversion, Software defined radio, AD9361, Decimation, Down Sampling, Low pass filters

I. Introduction

Software Defined Radio is a radio communication system where most of the physical layer functions are implemented by means of software on a PC or embedded system. The digital radio receiver section consists of fast ADC that converts RF signals to samples at high rate. But the signal of interest will usually be a small portion of the bandwidth. To extract the signal of interest from such high rate signals would require large filters. Digital down converter helps the frequency band of interest to be moved down the spectrum. This helps in reducing the sample rate and thus reducing filter requirements and simplifying signal processing.

II. DDC Design

Digital down conversion involves three steps such as frequency shifting, filtering and decimation. A high speed ADC converts the incoming analog signals into samples at high rate. Frequency shifting is usually carried out using a Direct Digital Synthesizer (DDS) which creates a complex sinusoid at the carrier frequency. The input real signal is multiplied or mixed with the carrier frequency, creating images centred at the sum and difference frequencies. The low pass filters reject the high frequency signals or the sum frequency and passes the baseband or difference frequency, thus producing a complex baseband representation of the original signal. Now we have a low frequency baseband signal sampled at a very high frequency which may lead to complex processing. Hence the signal is down sampled using decimators which retain some samples and discards other samples at regular intervals. Figure 1 shows a basic DDC block diagram.

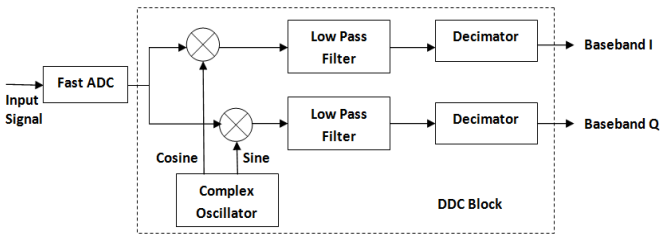

Figure 1: DDC Block Diagram

III. DDC Design using AD9361 Transceiver

The AD9361 is a highly integrated RF agile transceiver with high programmability and wideband capability, making it suitable for a broad range of transceiver applications. It consists of an RF front end, flexible mixed-signal baseband section, integrated frequency synthesizers and a configurable digital interface to a processor. It operates in the 70 MHz to 6.0 GHz range and supports channel bandwidths from less than 200 kHz to 56 MHz. It supports TDD and FDD operations. It consists of 6 differential or 12 single-ended inputs and 4 differential outputs with integrated 12-bit DACs and ADCs.

The RX section of AD9361 consists of two independent direct conversion receivers with features such as independent automatic gain control, dc offset correction, quadrature correction and digital filtering, thus eliminating the need for these functions in the digital baseband. Two high dynamic range ADCs per channel digitize the received input signal and pass them through configurable decimation filters and 128-tap finite impulse response (FIR) filters to produce a 12-bit output signal at the appropriate sample rate. The sample rate of each digital filter block is adjustable by changing decimation factors to produce the desired output data rate. The filters are programmed via SPI (Serial Peripheral Interface) registers.

IV. DDC Design Implemented in SOC

A comparative study on the various digital filters used for DDC is conducted and a suitable DDC design is implemented on SOC for the SDRP.

A. FIR versus IIR filter

FIR filters are filters whose impulse response is of finite duration, because it settles to zero in finite time. Such filters require no feedback; hence the implementation is simple and also any rounding errors are not compounded by summed iterations. They are inherently stable and have linear phase characteristics. But it requires more computation power compared to an IIR filter with similar sharpness or selectivity; they use addition, subtraction, but most FIR filters also require multiplication. FIR filters have a well defined frequency response but they require lot of hardware to store the filter coefficients. A comparison of the FIR and IIR filter is shown in Table 1.

TABLE I : FIR VERSUS IIR FILTER

FIR FILTER	IIR FILTER
Impulse response is of finite duration	Impulse response is infinite
Output depends on previous input samples.	Output depends on previous inputs and outputs.
Have linear phase characteristics	Dont have linear phase characteristics
Require more memory	Require lesser memory
Easier to implement	Difficult to implement

B. CIC versus FIR filter

CIC filters are an optimized class of finite impulse response (FIR) filter combined with an interpolator or decimator. CIC filters require no multiplications. They are coefficient less so hardware requirement is much reduced. Using CIC filters can cut costs, improve reliability and help performance. But they don't have a well defined frequency response. Hence, a follow-on FIR filter is used at the output of CIC which operates at reduced clock rates, minimizing power consumption in high-speed hardware applications.

For large rate changes, a CIC has a significant advantage over a FIR filter with respect to architectural and computational efficiency. Where only a small amount of interpolation or decimation are needed, FIR filters are more economical. The frequency response is well defined for FIR filter when compared to CIC. CIC requires a compensation filter at its output to meet the spectral requirements which may contribute to filter complexity thus contributing to the cost. Hence, for low decimation rates, CIC filter is not very optimal. A comparison of CIC and FIR filter is shown in Table 2.

TABLE 2
CIC VERSUS FIR FILTER

CIC FILTER	FIR FILTER
Have low pass frequency characteristics	Have low pass,high pass and band pass frequency characteristics
Use only addition and subtraction	Also require multiplication
Have a specific frequency roll-off	Arbitrary sharp frequency roll-off
Significant advantage over FIR filter for large rate changes.	More economical for small rate changes.

Thus FIR filter is suitable for low amounts of decimation or a CIC filter followed by an FIR filter for larger downsampling ratios.

V. Work Done

For this SDR application, AD9361 is used as the transceiver. The baseband signal arrives at the receiver section of the IC, where it passes through two programmable analog low-pass filters, 12-bit ADC and four stages of digital decimating filters. A decimation of upto a factor of 48 can be achieved within this IC. Any further decimation required according to the application, is programmed accordingly on a filter structure designed and implemented on SOC. This is achieved using an FIR filter and decimator structure for low decimation rates and for high decimation rate, a cascade of CIC and half band filter is used thereby utilizing the advantages of both the filters. The filters of AD9361 and SOC are programmable and any of the filters can be bypassed thus providing the flexibility of choosing appropriate decimation rates. The output signal is then passed to PC for processing via Ethernet or PCI express.

VI. Conclusion

An efficient Digital Down Converter for an SDR platform has been designed offering significant benefits in performance, density and cost. Together with the benefits of using AD9361 transceiver for the SDR application, an optimal DDC design implemented on SOC provide additional flexibility in selecting the appropriate decimation rate according to the required application. Since the filters of AD9361 as well as the DDC on SOC are programmable from the PC, the end user can choose an appropriate combination of decimation rate on each, suitable for his application. By conducting comparative studies on the various digital filters, an optimum design for DDC on SOC is selected and implemented. Proper selection of decimation filters used for data rate conversion as well as filtering in DDC is required as they play a key role in determining the efficiency of the overall hardware.

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