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Analyzing Performance of VHDL-AMS for Switch Level Modeling and Simulation

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Abstract— ***VHDL-AMS (IEEE 1076.1-1999), an extension to the VHDL, is considered to be a unified language for digital analog, mixed-signal modeling [1],[2]. Although traditionally AMS language is commonly used for behavioral modeling, in this paper special emphasis is given to modeling of mosfet based devices at switch level. We have analyzed VHDL-AMS for switch level modeling on basis of accuracy and response time. It is demonstrated by comparing parameters of CMOS inverter, universal gates and full adder. For all circuits implemented at switch level mosfet used is level-3 MOS Empirical model validated in SystemVision 5.9 from Mentor Graphics***

Keywords—VHDL-AMS, modeling, MOSFET, simulation

I. INTRODUCTION

VHDL-AMS (IEEE 1076.1-1999) was originally developed to describe event-driven systems [3]. With this extension, VHDL-AMS can describe and simulate digital, analog, and mixed-signal systems. In this paper it will be shown that this new standard is of big interest not only for circuit and system description but also for modeling of semiconductor devices. This paper exploits the rich expressiveness of VHDL-AMS for describing semiconductor devices. This paper exploits the rich expressiveness of VHDL-AMS for describing semiconductor devices. Before a device can be used for circuit design, its behavior must be correctly described by a device model, which is a set of mathematical equations. In this paper, VHDL-AMS is used to describe and implement MOS level-3 Empirical model for 1um technology. This device model is used to develop CMOS inverter, universal gates- NAND, NOR and full adder.

The paper is organized in following manner- 1.In the second section we first discuss the most significant features of VHDL-AMS. 2. In section III, we present VHDL-AMS modeling of a MOS level-3 with its characteristics using System Vision.3. In section IV, we have discussed the results based on the voltage transfer characteristics of switch level CMOS inverter. This section also describes, the universal gates synthesized using MOS device model created using VHDL-AMS and examines performance of switch level modeling with behavioral modeling for full adder circuit in VHDL-AMS. 4. Finally section V discusses the simulation results and draws some conclusions.

II. BRIEF DESCRIPTION OF VHDL-AMS

The VHDL-AMS language supports the description of analog electronic circuits using Ordinary Differential Algebraic Equations (ODAEs), in addition to its support for describing discrete-event systems [3], [4]. In comparison to traditional analog description languages, such as SPICE, the VHDL-AMS allows mixed analog/digital hardware descriptions on different levels of abstraction ranging from transistor to system level; VHDL-AMS is designed to fill a number of needs in the design process. The advantage of this language is that each subsystem can be designed independently of others. When one uses a subsystem, it can be thought of as an abstraction rather than having to consider its detailed composition. So at any particular stage in the design process, attention is given to the small amount of information relevant to the current focus of design. In an attempt to support the modeling and simulation of nonelectrical systems as well, several modeling methods using energy equivalences between the electrical domain and other domains, such as mechanical, thermal, or fluidic domains, mixed signal language have been proposed[5]. A large variety of modern applications is implemented using mixed analog digital circuits on a single silicon chip system on chip (SoC). The approval of VHDL-AMS as the IEEE standard for describing and simulating mixed systems is further evidence of the need for an integrated tool allowing the modeling, the simulation, or the virtual prototyping of heterogeneous systems on a chip.

III. MODELING OF LEVEL-3 MOS

The modeling process of MOS level-3 model is described in this section. MOS level-3 models are precursors to newer MOS models. Overall, the MOS level-3 model is an empirical device model. Level-3 models requires less simulation time, provides as much accuracy as level 2, and have a greater tendency to converge[6]. Some parameters defined for level-3 MOS are:

KAPPA – Saturation field factor. It is an empirical factor in the equation for the channel length in saturation.

ETA –Static feedback on VT. Models effect of VDS on VT, i.e., DIBL (Drain-Induce Barrier Lowering)

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THETA – Mobility modulation, it models the effect of VGS on surface mobility.

The VHDL-AMS model of MOS level-3 was designed in the following stages: Entity declares the parameters considered for level-3 it assigns default values which can be changed as per user requirement and terminals of the model. The MOS-3 entity has four terminals-drain, gate, source and bulk are also declared. Architecture definition describes the model evaluation procedure. The computation of important quantities, such as drain currents and charges, are carried out in this section. In general, VHDL-AMS processes the model parameters and then computes the drain currents and charges. Constants like epso, Ni, Boltzmann, epsSiO2 and q are defined. Quantities like Vdsq-drain to source voltage, Vgsq, Vbsq; Idq-current through drain, Isq, Ibq are also declared. Finally, total currents flowing into each terminal are computed by combining static (dc) currents and dynamic (e.g., time derivative of charges) currents. The various parameters required to calculate the drain current are computed in the architecture. The model parameters used are extracted from the spice datasheet. Some of those parameters directly relate to the semiconductor process, e.g., doping and oxide thickness [7]. The mosfet pseudo code is given below in figure 1.

```
library IEEE;
use IEEE.math_real.all;
use IEEE.electrical_systems.all;

entity mosfet is
    generic(
    width   : real:=1.0E-6;
    length  : real:=1.0E-6;
    channel: real :=1.0;
    -- +1 for NMOS, -1  for PMOS
    vt0     : real:= real'low;
    kp      : real:= 2.0E-5;
    gamma   : real:= 0.5276;
    tox     : real:= 1.0E-7;
    nsub    : real:= 1.0E15;
    .
    .
    u0      : real:= 600.0;
    --600 for NMOS, 250 for PMOS
    kappa   : real:= 0.2;
    ngate   : real:= 1.5e19;
    Temperature : real :=300.0
    );
    port(terminal drain,gate,source,bulk: electrical);
end entity ;

architecture moslevel3 of mosfet is
  quantity Vdsq across drain to source;
  quantity Vgsq across gate to source;
  quantity Vbsq across bulk to source;
  quantity Idq through drain;
  .
  .
End architecture moslevel3 ;
```

Fig 1.VHDL-AMS level-3 MOS model

Following are the symbols generated in SystemVision using symbol generation tool for NMOS and PMOS models. The figure 2 and 3 demonstrate the PMOS and NMOS symbols generated respectively. These symbols are used in further implementation of circuits.

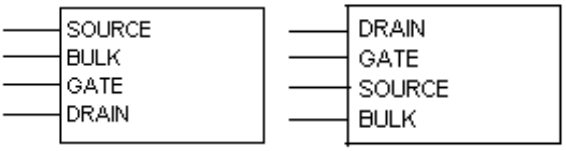

Fig 2.PMOS symbol Fig 3.NMOS symbol

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IV. RESULTS AND DISCUSSIONS

A. Simulation results for MOSFET model:

The mosfet model developed is validated from the input and output characteristics of mosfet. Simulation results for mosfet output (ids vs vds) and input (igs v svgs) characteristics are shown in figure 4 and 5 respectively.

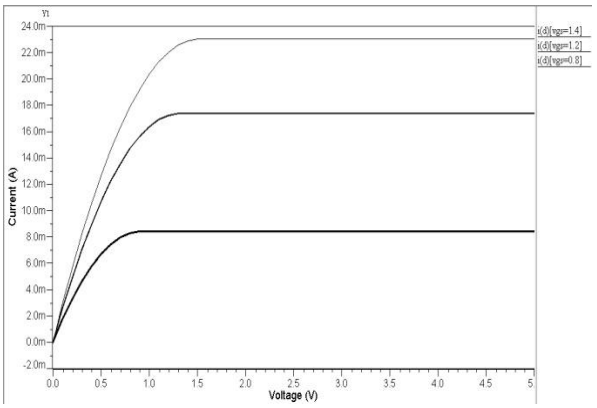

Fig 4.Output characteristics (id vs vds)

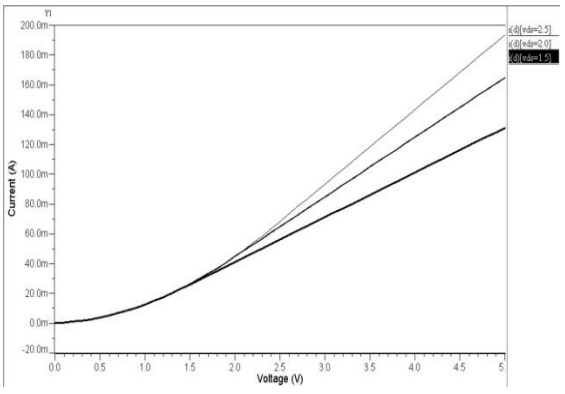

Fig 5. Input characteristics (ig vs vgs)

B..CMOS Inverter

The CMOS inverter is designed using level3 NMOS and PMOS model, and the results are verified with CMOS inverter using SPICE (Aimspice). The results obtained from the comparison of voltage transfer characteristics of VHDL-AMS model and SPICE model are found to be similar. Figure 6 demonstrates the CMOS inverter generated using mosfet model generated in VHDL-AMS. Figure 7 illustrates the voltage transfer

characteristics (vtc) or the output voltage (vout) vs the input voltage (vin).

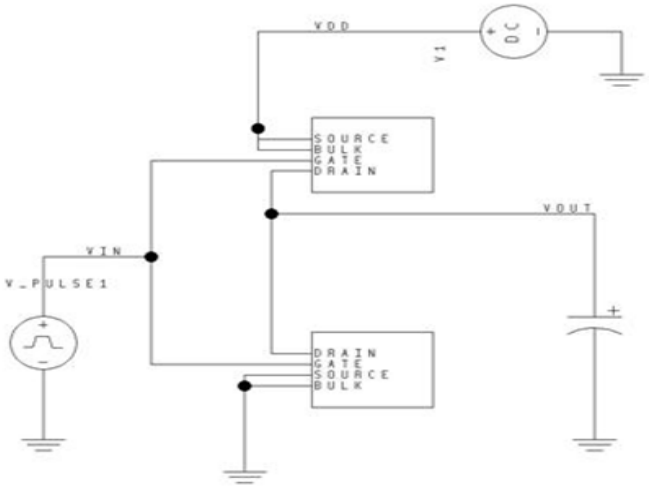

Fig 6.CMOS inverter circuit

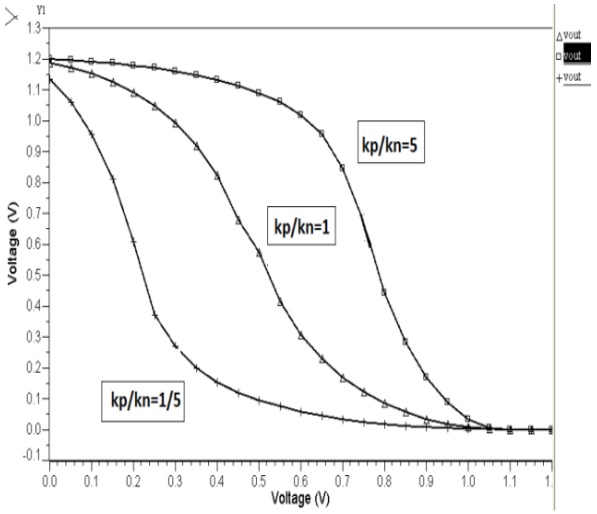

Fig 7. CMOS voltage transfer characteristics

\For lower values of ratio kp/kn, full swing in output voltage from ground to Vdd (1.2V) is not obtained. This indicates that aspect ratio for pmos should be more compared to that of nmos for proper operation of CMOSinverter. Hence switch level cmos inverter generated using mosfet model in SystemVision is validated.

C. Implementation of universal gates

Any digital circuit can be designed by using universal gates either nand or nor. We have demonstrated NAND and NOR circuits using switch level modeling in VHDL-AMS. Again switch level refers to level-3 MOS specified in Section III. The NAND operation is implemented as shown in figure 8 with the respective the output waveform shown in figure 9. The NOR operation is performed using mosfet model as illustrated in figure 10 with its output waveform shown in figure 11.

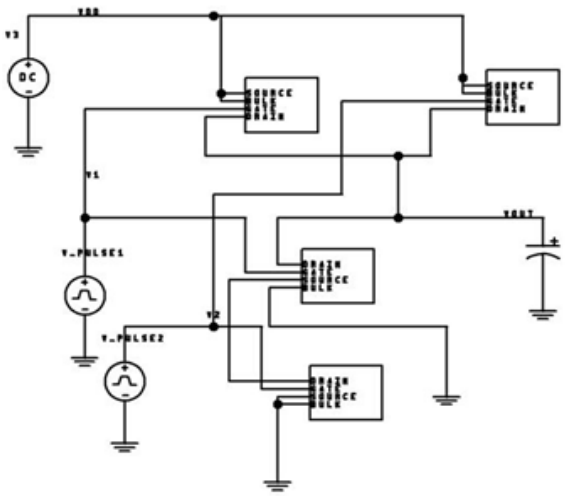

Fig 8. NAND gate circuit

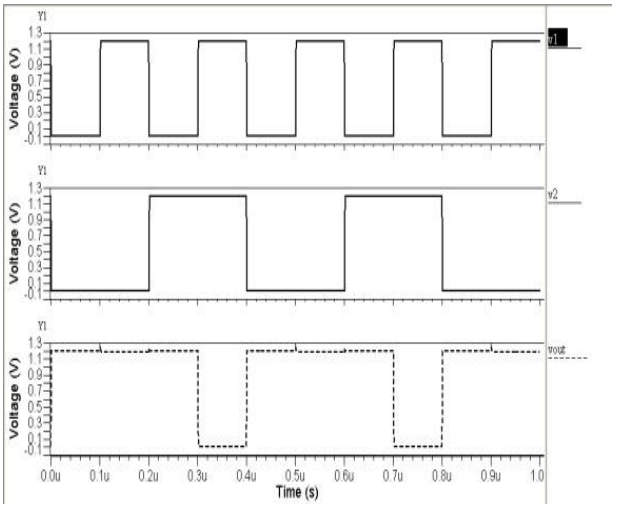

Fig 9. NAND simulation waveforms

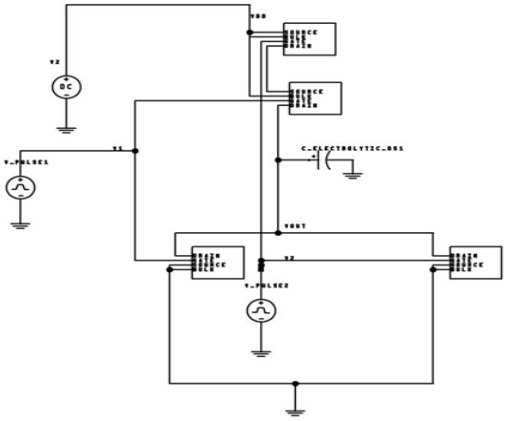

Fig 10. NOR gate circuit

The waveforms obtained from the simulation of NAND, NOR switch level circuits match with the actual output waveforms of NAND, NOR logic gates.

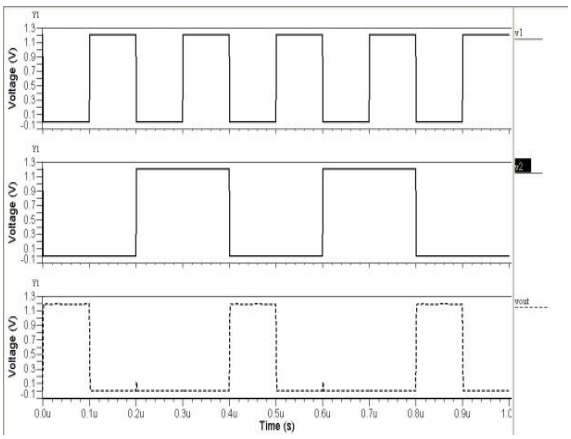

Fig 11. NOR simulation waveforms

D. Comparison between switch level and behavioral modeling

In this section, we have implemented full adder circuit using switch level modeling and behavioral modeling. The comparison is done between both modeling techniques based on performance and speed of simulation. The circuit implemented to perform full adder using NAND model is shown in figure 12. The output waveforms obtained during simulation of sum and carry along with the inputs are shown in figure 13.

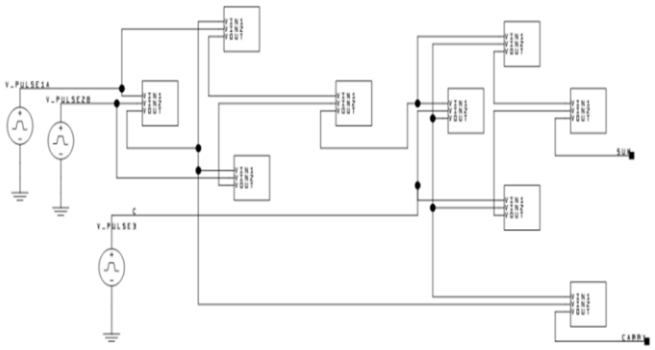

Fig 12. Full adder circuit using NAND gates

The full adder circuit comprises of nine NAND gates. The NAND gate used for the purpose was modeled from level-3 MOS given in section IV. Thus we have used indirect switch level modeling through gate level modeling.

TABLE I : COMPARISION BETWEEN SWITCH LEVEL AND BEHAVIOURAL MODELLING OF FULL ADDER CIRCUIT

Parameter	Switch level modeling	Behavior modeling
CPU Time	2.2 sec	16 ms
Length of code	More	Less

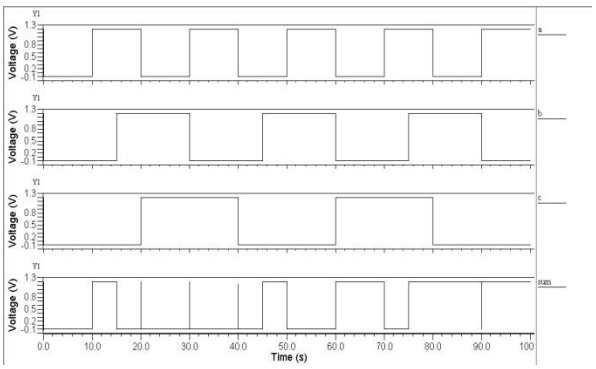

Fig 13 . Full adder characteristic for switch level modeling

For switch level modeling speed is reduced due to increased complexity [8]. As each NAND gate is developed with four mosfet and nine such NAND gates are used to implement the Full adder so the overall complexity is boosted. The spikes in output are observed due to transition in input pulses. Figure 14 demonstrates the behavioral code designed for 3-input full adder. Behavioral code for 3-input full adder is as shown below.

```
library ieee;

use ieee.std_logic_1164.all;

 entity full_adder is

   port (

      in1, in2 ,in3 : in  std_logic;

      s , c  : out std_logic);

 end entity full_adder;

 architecture fa of full_adder is

   begin

   s <= in1 xor in2 xor in3  ;

   c<= (in1 and in2) or (in2 and in3) or (in3 and in1);

 end architecture fa;
```

Figure14. Behavioral code for full adder

CPU time of behavior modeling is less compared to the switch level modeling as shown in Table 1. In switch level modeling extra time is required to call each MOSFET model from test bench which is not required for behavior modeling. Switch level modeling is better for practical analysis of circuit as it considers all the performance parameters; while behavioral modeling emphasizes on predicting ideal responses based on behavioral equations.

V. CONCLUSION

The various examples demonstrated highlights that VHDL-AMS is well suited for modeling of semiconductor devices. Conventionally VHDL-AMS is preferred for behavioral modeling. However this paper focuses on switch level modeling

aspect of VHDL-AMS language. Experimental results show that the responses of circuits derived from VHDL-AMS switch level models corresponds well with the actual responses for the same logic circuits. This suggests that VHDL-AMS can be used to implement switch level device modeling at cost of execution time. The experiments can be further carried out for modeling of mixed signal circuits at switch level and behavioral level using VHDL-AMS.

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