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Switching Techniques: Concepts for Low Loss Switching

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Abstract- Highlighting the dominance & supremacy of CMOS digital logic design over its counterparts & further coming up with a unique solution to minimize the power losses prevalent in switching implementations using CMOS, this brief introduces a novel SDLC (Switching-Diode-Inductor-Capacitor) design. It presentsa design which in ideal case may lead to a circuit capable of performing logic operations with no switching losses. In traditional CMOS logic design, energy is stored in a load capacitor when the output is high & it dissipates this stored energy during low level output. Attempt has been made to harness this discharging energy by storing it inside an inductor in the form of magnetic fieldin the proposed SDLC architecture. This significantly reduces the switching dissipation energy. The proposed SDLC architecture has been illustrated via MULTISIM software simulation. A brief description of existing logic design implementations and scope for future research in this domain has also been discussed in this paper.

Keywords-SDLC(Switching-Diode-Inductor-Capacitor); architecture; implementations; CMOS; design; dissipation; energy.

1.INTRODUCTION

The current trend towards low-power design is mainly driven by two forces [1]: thegrowing demand for long-life autonomous portable equipment and the technologicallimitations of high-performance VLSI systems. For the first category of products, lowpower is the major goal for which speed and/or dynamic range might have to be sacrificed.

High speed and high integration density are the objectives for the second applicationcategory, which has experienced a dramatic increase of heat dissipation that is nowreaching a fundamental limit. These two forces are now merging as portable equipmentgrows to encompass high-throughput computationally intensive products such as portablecomputers and cellular phones.The most efficient way to reduce the power consumption of digital circuits isdefinitely to reduce the supply voltage, since the average power consumption of CMOSdigital circuits is proportional to the square of the supply voltage. On the other hand, thereduction of the supply voltage is also required to maintain the electric field at anacceptable level. The resulting performance technologies by introducing more parallelism (AND / OR) modify the process andoptimize it for low supply voltage operation.

Standard CMOS Low loss switching technique provides the power supply function through low loss components & the use of switches that are in one of two states, on or off. The advantage is that the switch dissipates very little power in either of these two states and power conversion can be accomplished with minimal power loss, which equates to high efficiency.

Electrical & Electronic Switches: Electrical switches are basically mechanical switches, which make or break an electrical contact when some force either manual or magnetic, is applied to move the switch to an on or off position. Toggle switches have a lever which is pushed or pulled, like the common light switch. Power windows and locks in automobiles use rocker switches. which rock back and forth when pressed. Keyboard switches are found on computers washers, stoves and other devices with push controls. Electronic switches are electrical switches which do not have mechanical contacts, but use semiconductor devices. These switches apply electrical control signals to terminals on the switch which opens and closes the contacts. Electronic switches are available in a vast range of configurations such as toggle, rocker, push button, rotary, slide, and reed and relay switches.Since power dissipation is a prime design constraint; low-power design requires operation at lowest possible voltage and clock speed & it requires optimization at all levels of abstraction. With the continuous scaling of the technology, the power consumption has become a bottleneck for widely used high-speed, battery powered portable devices. The proliferation of portable and hand-held electronics combined with increasing packaging costs is forcing circuit designers to adopt low power design methodologies incorporatinglow loss switching techniques. It is the aim of this paper to present a novel low-power logic design scheme incorporating low loss switching technique.

In the subsequent paragraphs CMOS technology that has played an increasingly vital role in the global integrated circuit industry is dealt in depth outlining its advantage & supremacy over switching implementation utilizing NMOS/PMOS, BJT's, FET's ,SCR's, etc. Power dissipation in a CMOS-based logic circuit is dominated by the switching energy [1][2]. This is the energy that must be dissipated in order to change internal state of the devices. Other sources of energy loss in CMOS circuit are related to leakage current [3][4] and to the short-circuit current [2][5]. While the other two types of energy loss can be reduced to arbitrary low levels (at least in theory) by regulating the voltages levels (both power supply and thresholds), there seems to be no solution to eliminate dynamic power dissipation [1].

CMOS v/s NMOS and PMOS: A traditional CMOS logic gate consists of N- channel network (pull-down network) and a complementary P- channel Network (pull-up network).PMOS can efficiently drive high voltage, or logic one value, and NMOS transistors, are good at driving a zero voltage. The presence of complementary transistors allows CMOS logic gates to be implemented so that the output voltage level is connected to the power or ground line, but not to the both simultaneously so the gate will work correctly no matter what

the width to length ratio of the transistor is. Traditional CMOS gates are known as RATIOLESS LOGIC gates. The main advantage of CMOS implementations were -reduced standby power by six order of magnitude over equivalent bipolar and PMOS implementations, they also possess good noise margins [6]. Other advantages of static CMOS logic style are its robustness against voltage scaling and transistor sizing and thus ensuring reliable operation at low voltages and arbitrary transistor sizes [6]. The major drawback of CMOS circuits are that the total number of transistors used are 2N, where N being the number of transistors in N- channel network [7]. Also as the number of input lines increases the number of series connection of PMOS transistors increases and leads to increase in switching time. NMOS or Pseudo NMOS logic gates are realized by replacing the pull up network by a single P- channel transistor used as the load for each logic gate or by an N- channel depletion transistor used as a load resistor. These logic gates are known as RATIOED LOGIC gates.This greatly simplifies and shrinks the circuit by nearly half the number of transistors used in CMOS gates. However these have a greater disadvantage that they dissipate power even when their outputs are not changing, i.e. their static power dissipation is not zero. Also they are slow in comparison with CMOS gates.

CMOS v/s BJT's,FET's, SCR: BJT's and FET's also find their application in switching circuits. Transistor switchescan be used for controlling high power devices such as motors, solenoids or lamps, but they can also be used in digital electronics and logic gate circuits. Both the NPN & PNP type bipolar transistors can be made to operate as "ON/OFF" state and function like an electronic switch by controlling base current. Like its bipolar cousin, the field-effect transistor may be used as an on/off switch controlling electrical power to a load. It can be made to function like a switch by controlling the current flow through the channel by a control voltage applied at the Gate terminal.We also have another class of Power Semiconductor Devices which can be used as switches. Thyristor is the general name given to a family of semiconductor devices having four layers with a control mechanism. They basically serve in electronic switching. SCR (Silicon Controlled Rectifier) is one such example of a power semiconductor device which has wide range of application in switching. Transistors and Thyristors are both semiconductor devices, now widely employed in switching operations because of their numerous advantages such as noiseless operation, very high switching speed, high efficiency, small size, light weight and trouble free service for a long period. However in context to present scenario of demand for low power dissipation while switching, MOSFET's have dominated the market. With zero power dissipation in standby mode they have ruled out the market place for other semiconductor devices as electronic switches. Also MOSFETs being majority carrier devices, can switch very quickly (100's of kHz to over a MHz).The Bipolar transistors when operated in the linear region have been most beneficially used in high current drive circuits exploiting it's speed & have surpassed MOSFET's dominance. However, when operated in the saturation region bipolar power transistors require the supply and removal of stored charge during each switching cycle, resulting in extended turn-off delay times.

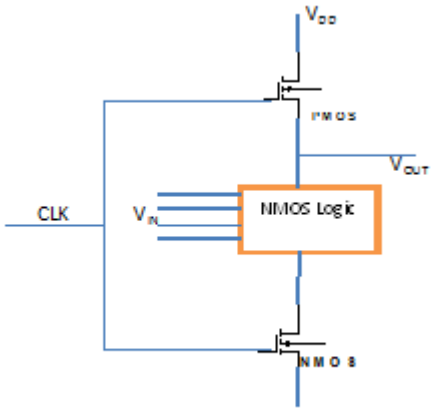
Power Estimation

The power dissipation of a logic gate may be broadly categorized into static and dynamic power. Static power involves dissipation when logic gate is not switching. Dynamic power involves the power during switching operation.

Dynamic Power: $P_{Dynamic} = \alpha C_L V^2_{DD} F_{CLK}$ **Static Power:** $P_{Static} = (I_{DC} + I_{Leckage}) * V_{DD}$ **Total Power:** $P_{Total} = P_{Static} + P_{dynamic}$

II.EXISTING LOGIC DESIGNS*Dynamic CMOS Logic Design*

Dynamic logic (or clocked logic) is a design methodology in combinatorial logic circuits. It is distinguished from the so-called static logic by exploiting temporary storage of information in stray and gate capacitances. Dynamic logic circuits are usually faster than static counterparts, and require less surface area, but are more difficult to design, and have higher power dissipation. Static logic is slower because it has twice the capacitive loading, higher thresholds, and uses slow p-transistors for logic. Dynamic logic can be harder to work with, but it may be the only choice when increased processing speed is needed. In general, dynamic logic greatly increases the number of transistors that are switching at any given time, which increases power consumption over static CMOS

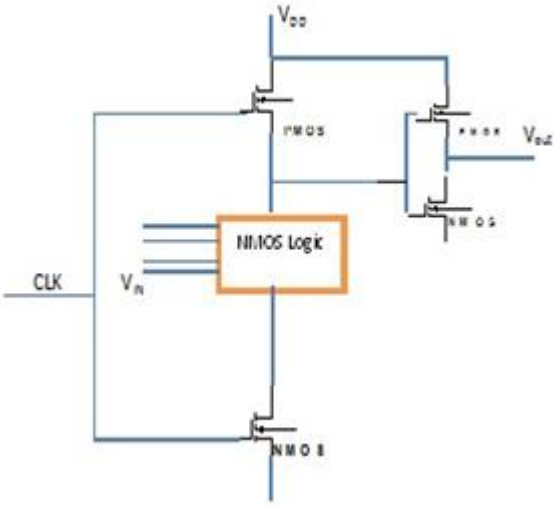


Differential CMOS design

In differential logic design, each input is represented by the voltage difference between two wires. One wire will be denoted by the positive and the other will be denoted by negative. If the voltage on first wire is greater than the voltage on the second wire, the signal is considered to be 1, otherwise 0. Some of the advantages of differential CMOS logic design include, (a) Logic inversions are simply obtained by interchanging the wires without incurring a time delay. (b) Load network consists of two cross coupled p-channel transistors only. This minimizes both the surface area and the number of series of p-channels transistors compared to conventional CMOS logic designs. (c) They are less sensitive to noise corruption. However the biggest disadvantage is that we have to use two wires to represent every signal.

Dominos CMOS Logic Design

Domino logicis a clocked logic family, which means that every single logic gate has a clock signal present. It overcomes the main drawback in dynamic logic & thus unrestricted cascade operation is possible. Addition of inverters allow us to operate a number of structures in cascade [7]. It utilizes smaller areas compared to conventional CMOS logic & operation is free of glitches since each gate can make one transition.



CMOS Adiabatic Circuits

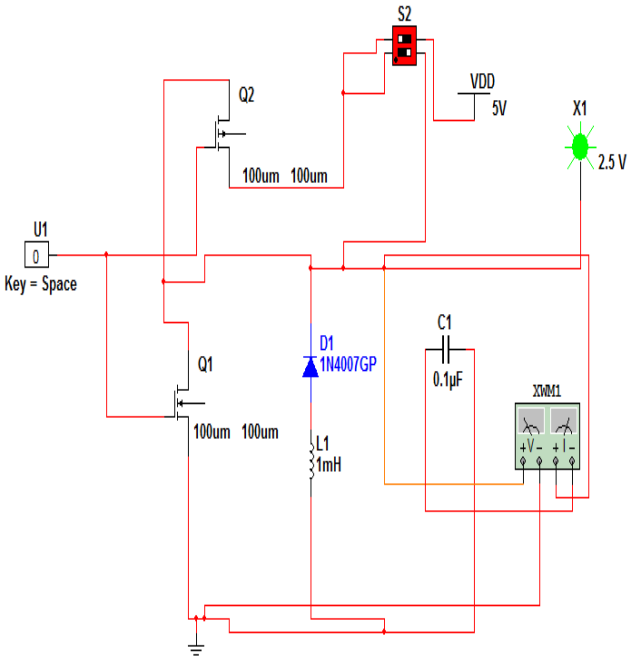
Adiabatic logic works with the concept of switching activities which reduces the power by giving stored energy back to the supply. It is a classical approach to reduce the dynamic power. Though it does not fit enough to meet today's power requirement. However, most research has focused on building adiabatic logic, which is a promising design for low power applications. Thus, the term adiabatic logic is used in low-power VLSI circuits which implements reversible logic. There are several important principles that are shared by these low-power adiabatic systems. These include only turning switches on when there is no potential difference across them, only turning switches off when no current is flowing through them, and using a power supply that is capable of recovering or recycling energy in the form of electric charge. To achieve this, in general, the power supplies of adiabatic logic circuits have used constant current charging in contrast to more traditional non-adiabatic systems that have generally used constant voltage charging from a fixed-voltage power supply. The power supplies of adiabatic logic circuits have also used circuit elements capable of storing energy. This is often done using inductors , which store the energy by converting it to magnetic flux, or, as in case of Asynchrobatic Logic, by using capacitors, which can directly store electric charge.

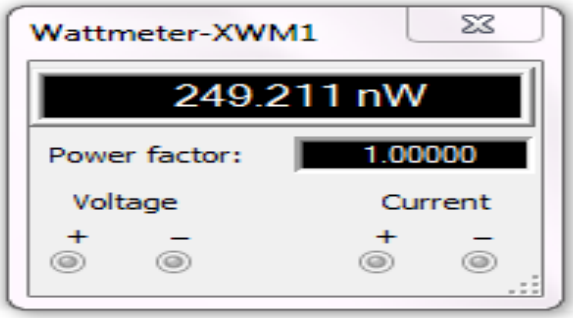
III. PROPOSED LOGIC DESIGN

***Switching Diode Inductor Capacitor (SDLC) architecture*:**The idea proposed here is simulated using MultiSim Software by National Instruments. The simulation of the theorized idea is done using simple CMOS NOT gate. It is based on the energy exchange in the Switching, Diode-Inductor–Capacitor (SD*LC*) circuit. In conventional integrated circuit design, the energy is stored in the output load capacitor through a pull-up path (corresponding to storing a logic 0). When the output changes its logic value, this stored energy is dissipated through the pull down path to the ground. In order to reduce this switching energy dissipation each time the load capacitor is discharged, its energy is stored in the magnetic field of the inductor in the proposed SD*LC* architecture. Whenever the output load needs to be charged again, the energy is transferred back from the inductor to the load capacitor. The diode here prevents the reverse path followed by the current to discharge the capacitor by shorting the NMOS transistor.

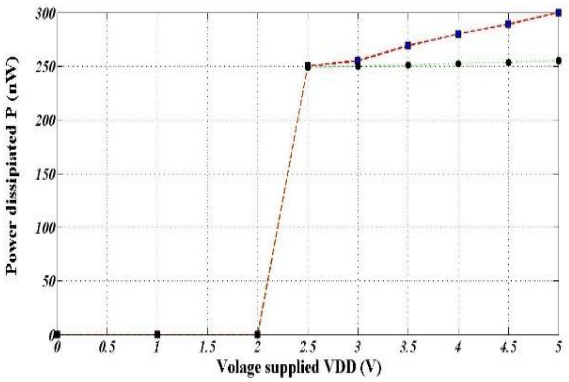
This significantly reduces the switching energy. Thus it presents a design scheme which in ideal case may lead to a circuit capable of performing logic operations with minimum switching losses. Moreover, the voltage across the fully charged capacitor (corresponding to logic 0) & across the inductor (corresponding to logic 1) is given as feedback voltage substituting the supply voltage V_{DD} (applied to the source of the p-mos transistor) till the value of the feedback voltage is comparable to V_{DD}. Once this feedback voltage drops to a significant value below V_{DD} through an appropriate switching mechanism the feedback voltage is replaced by the supply voltage V_{DD}& this way the transistor operation remains unaltered but the power dissipation gets significantly reduced. The switch represented in the simulation model is designed using combinations of diodes which allow the voltages, V_{DD} and feedback voltage, to be compared.

The wattmeter is shown with the simulation result to depict the reduction in power when SDLC circuit is simulated against conventional circuit. The power loss in conventional circuit rises with the increase in the supply voltage and the frequency of input signal. However for the proposed SDLC structure the power loss remains constant with the increase in supply voltage. Also the switching time power loss is reduced. These reduction in power loss greatly reduces the static power loss in CMOS switching circuits.





The simulation result is plotted using Matlab. The power supply in Volts (V_{DD})is plotted on X-axis and power dissipated in nanowatt (P) is plotted on Y-axis.



The graph shows an increase in power dissipated with increasing applied voltage in conventional design whereas the power dissipated remains constant with increased voltage in SDLC designed circuit.

IV.CONCLUSION

The design presented here in this SDLC architecture would dissipate least power (almost zero) under ideal conditions. Simulation results show correct behavior of proposed SDLC (Switching-Diode-Inductor-Capacitor) design. However to realize this technology on nanometer scale there are certain issues which are yet to be carefully analyzed and there is indeed a need for future research. Firstly, the placing of diode with inductor would increase the surface area required for designing the circuit. Moreover the diode will not behave ideally under real mode simulation. Secondly, the proposed architecture is beneficial for large capacitive loads. The SDLC architecture needs the fabrication of accurate inductors placed in series with diode. However this design greatly reduces the dynamic power consumption. The proposed architecture has been illustrated through MULTISIM software. The proposed architecture is especially suitable for circuits driving high capacitive loads, such as buses and clock distribution trees. Series practical issues such as non-ideal components, switch and fabrication of accurate inductors have to be addressed and dealt to make way for proposed architecture into digital designs.

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