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# Comparative Analysis of Three Topologies of Three-Phase Five Level Inverter

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***Abstract*—This paper presents the simulation and analysis of the three topologies of three phase 5-level inverter. We have considered the Flying Capacitor Multilevel Inverter (FCMLI), the Neutral Point Clamped or the Diode Clamped Multilevel Inverter (NPCMLI or DCMLI) and the Cascaded H-Bridge Multilevel Inverter (H-bridge MLI). The comparison between these inverters is based on the %THD present in the output voltage. Each inverter is controlled by the multi-carrier sinusoidal pulse width modulation (SPWM). The analysis shows that the total harmonic distortion (THD) is approximately 23% for DCMLI and 22% for PWM H-Bridge topologies, and it is about 24% for the FCMLI topology. The comparative results of the harmonic analysis have been obtained in MATLAB/SIMULINK.**

***Keywords*—Multilevel, Cascade, Harmonics, Modulation, MATLAB/SIMULINK, THD**

## I. Introduction

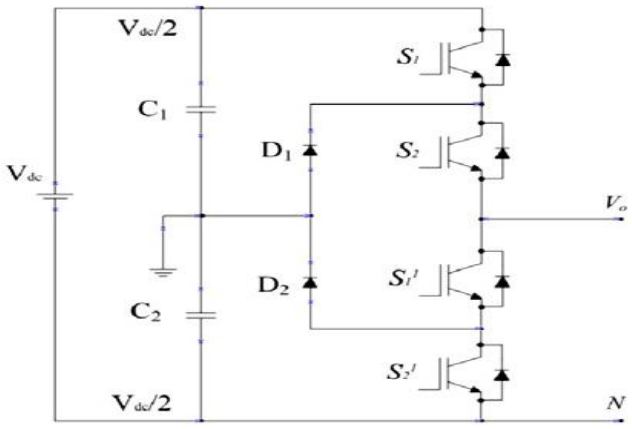
In the recent years, multilevel inverters (MLI) are increasingly being used for medium voltage and high power applications due to their various advantages such as low voltage stress on the power switches, low electromagnetic interferences (EMI), low dv/dt ratio to supply lower harmonic contents in the output voltage and current. Comparing two-level inverter topologies of the same power ratings, MLIs also have the advantages that the harmonic components of line-to-line voltages fed to the load are reduced owing to its switching frequencies [1].

In this paper, constant switching frequency multicarrier, sinusoidal pulse width modulation method is used for the multilevel inverter. Multilevel inverter is an effective solution for increasing power and reducing harmonics of an ac waveform. The control objective is to compare the reference sine wave with multicarrier waves for the three phase five level inverters. The elementary concept of a multilevel inverter to achieve higher power is to use a series of power semiconductor switches with several dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy sources can be used as the multiple dc voltage sources. The multilevel inverter output voltage has less number of harmonics [2, 3].

The most common MLI topologies are classified into three types: neutral point clamped (NPCMLI) or diode clamped MLI (DCMLI), flying capacitor MLI (FCMLI), and Cascaded H-Bridge MLI (CHBMLI). The basic topologies of the MLI are shown in Fig.1. The diode clamped inverters, particularly, the three-level structure have a wide popularity in motor drive applications besides other multilevel inverter topologies. However, it would be a limitation of complexity and number of clamping diodes for the DCMLIs, as the level exceeds. The FCMLIs are based on balancing capacitors on phase buses and generate multilevel output voltage waveform clamped by capacitors instead of diodes. The FCMLI topology also requires balancing capacitors per phase at a number of (m - 1) * (m - 2)/2 for an m-level inverter and it will cause to increase the number of required capacitor in high level inverter topologies and complexity of considering DC-link balancing [1].

Nowadays, the multilevel inverters have become more attractive for researchers and manufacturers due to their advantages over conventional three-level pulse width-modulated (PWM) inverters. They offer improved output waveforms, smaller filter size, low EMI, lower total harmonic distortion (THD). Multilevel inverter topology has the least components for a given number of levels. Cascaded H-Bridge-MLI topology is based on the series connection of H-bridges with separate DC sources. Since the output terminals of the H-bridges are connected in series, the DC sources must be isolated from each other. The need of several sources on the DC side of the inverter makes multilevel technology attractive for photovoltaic applications. Owing to this property, CHB-MLIs have also been proposed in order to achieve higher levels [1, 4, 5].

The Cascaded Multilevel

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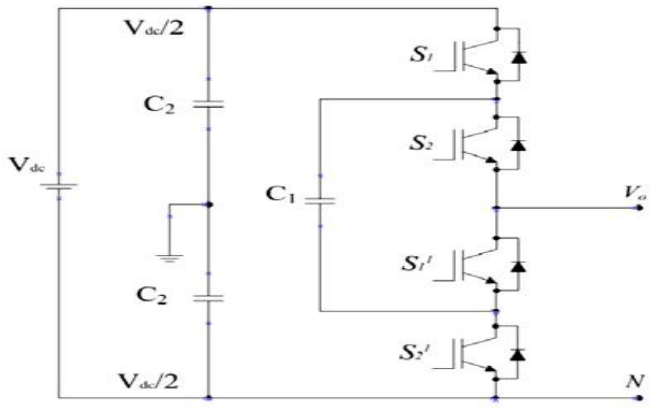


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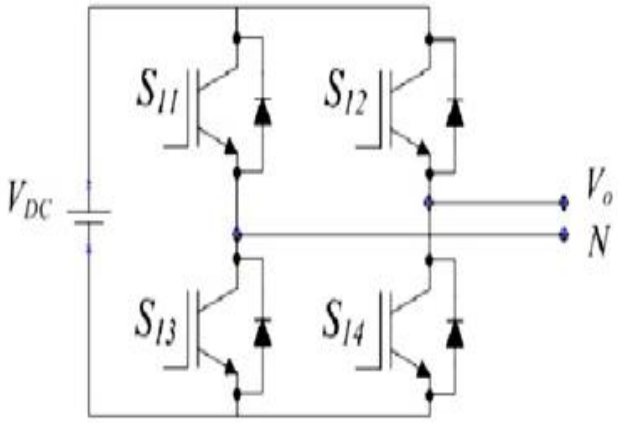



(c)

Fig.1. Multilevel inverter topologies: (a) three-level DC-MLI, (b) three-level FC-MLI, (c) three-level CHB-MLI. [1]

inverter is simply a number of conventional two-level bridges, whose AC terminals are connected in series to synthesize the output waveforms. The MLI needs several independent DC sources which may be obtained from batteries fuel cells or solar cells [6].

## II. Basic operating principle of Cascaded H –Bridge Multilevel Inverters (CHB-MLI):

The single phase 5-level Cascaded Multilevel Inverter consists of simple two H-bridge modules, whose AC terminals are connected in series to obtain the output waveforms Fig.2. shows the power circuit for a five level inverter with two cascaded cells. Through different combinations of the four switches of each cell, the inverter can generate FIVE different voltage outputs, +2 Vdc, + Vdc, 0, -Vdc, -2 Vdc . The number of voltage levels in a CHB inverter can be found from m = (2H+1) where H= is the number of H-Bridge cells per phase leg. The voltage level m is always an odd number for the CHB inverter. The total number of active switches (IGBT's) used in the CHB inverters can be calculated by $N_{sw}$ = 6(m-1) =6(4) =24 switches (for three phase) [6, 7]

The resulting AC output voltage is synthesized by the addition of the voltages generated by different H-bridge cells. Each single phase H-bridge generates three voltage levels as + Vdc, 0, - Vdc by connecting the DC source to the AC output by different combinations of four switches, S11, S12, S13, and S14 as seen in Fig 1.c) The CHB-MLI that is shown in Fig. 2 utilizes two separate DC sources per phase and generates an output voltage with five levels. To obtain +Vdc, S11 and S14 switches are turned on, whereas -Vdc level can be obtained by turning on the S12 and S13. The output voltage will be zero by turning on S11 and S12 switches or S13 and S14 switches. If n is assumed as the number of modules connected in series, m is the number of output levels in each phase as given by m=2n+1. The switching states of a CHB-MLI (sw) can be determined by using Eq. sw= $3^m$ [1].

Considering the simplicity of the circuit and advantages, Cascaded H-bridge topology is chosen for the presented work.

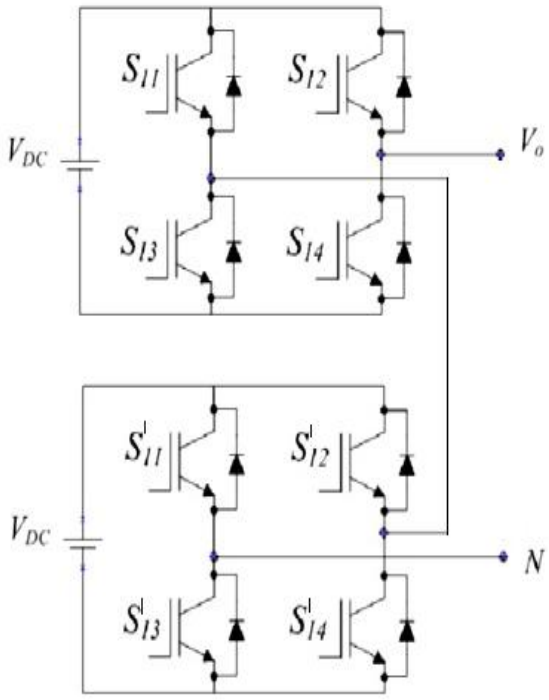



Fig.2. Single phase five level CHB-MLI. [1]

The three phase 5-level cascaded H-bridge inverter topology is realized using MATLAB/SIMULINK. The use of CHB-MLI reduces the total harmonic distortion (THD) in the output current waveform by increase in the number of levels of the output voltage. We can further increase the no. of levels of the inverter to reduce the harmonics. The proposed configuration reduces the THD of the current fed into the grid [8].

Fig.3. shows the three phase connection of a Cascaded H-Bridge multilevel inverter.

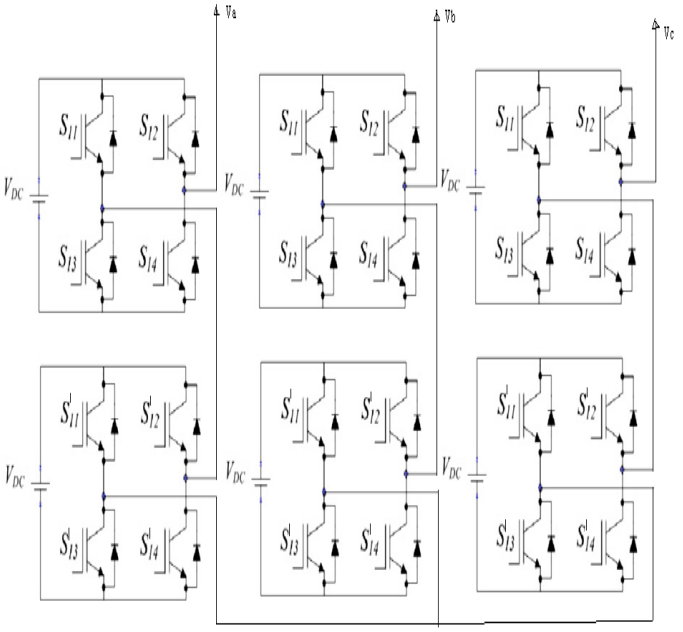
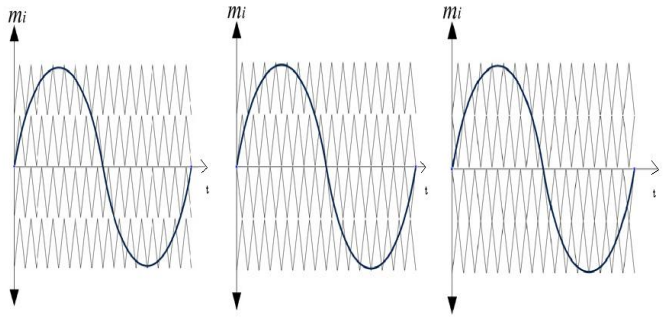



Fig.3. Three-phase five-level topology of Cascaded H-bridge multilevel inverter. [1]

## III. Control Technique

SPWM technique is one of the most popular modulation techniques among the others applied in power switching inverters. In SPWM control, a sinusoidal reference voltage waveform is compared with a triangular carrier waveform to generate gate signals for the switches of inverter. Power dissipation is one of the most important issues in high power applications. The fundamental frequency SPWM control method is proposed to minimize the switching losses. The multi-carrier SPWM control methods increase the performance of multilevel inverters and are classified according to vertical or horizontal arrangements of carrier signal. The vertical carrier distribution techniques are defined as Phase Dissipation (PD), Phase Opposition Dissipation (POD), and Alternative Phase Opposition Dissipation (APOD) as shown in Fig.4.[1]




(a) (b) (c)

Fig.4. Multi-carrier SPWM control strategies: (a) PD, (b) POD, (c) APOD [1]

## IV. Simulation and Results of the three topologies.

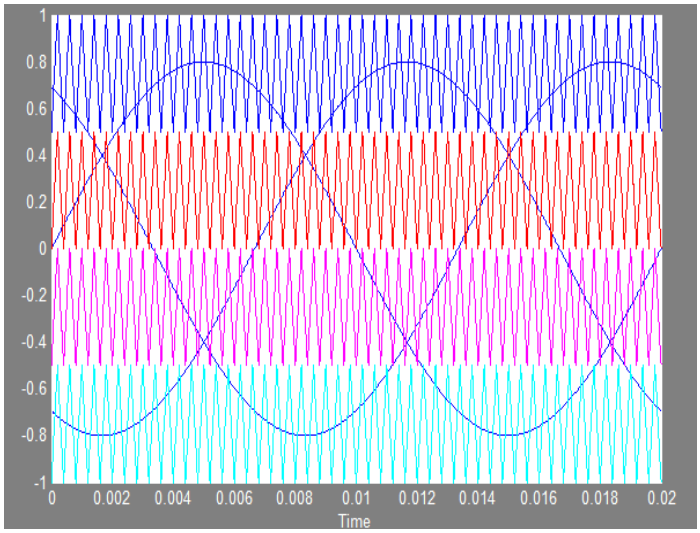



Fig.5. Simulation model for generation of pulses for one cycle ($M_a$=0.8, $f_m$ =50Hz, $f_{cr}$ =5 kHz)

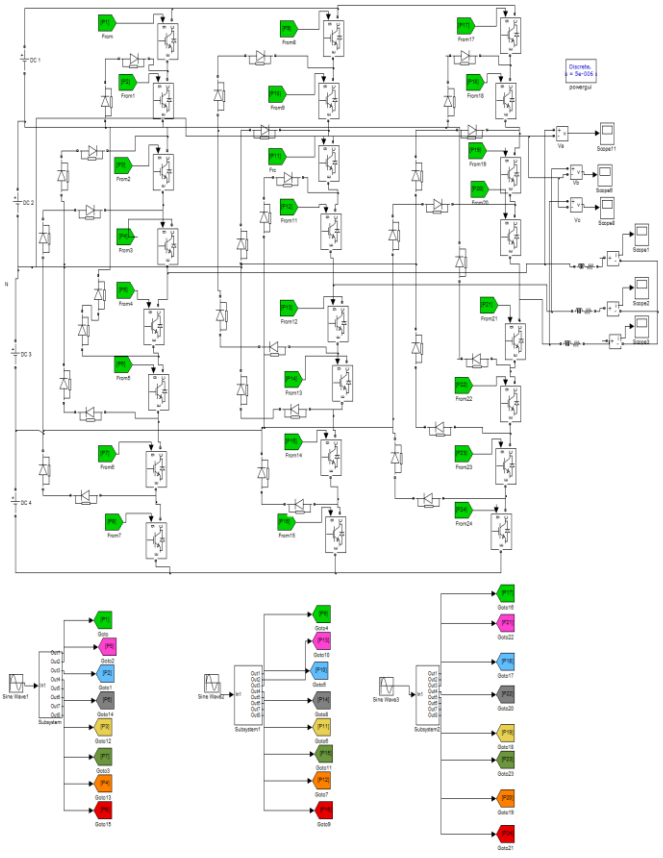


Fig.6.Simulink model of a three phase 5-level DC-MLI.

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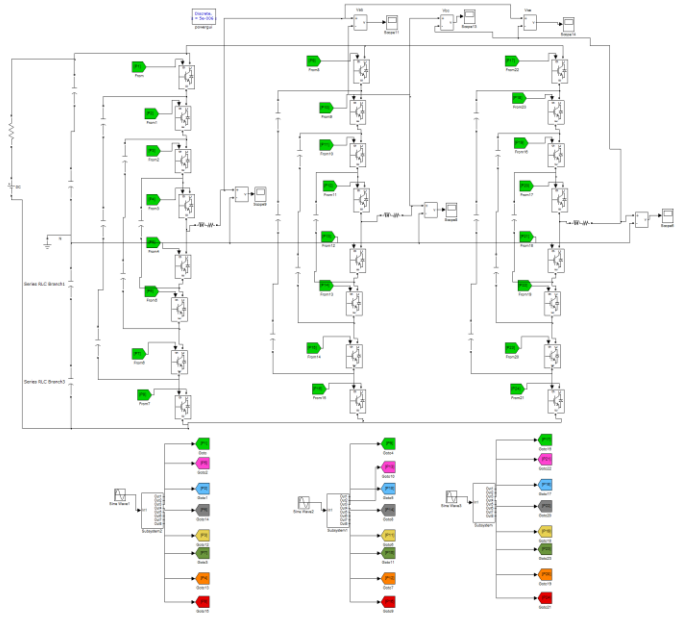

Fig.7.Simulink model of a three phase 5-level FC-MLI.

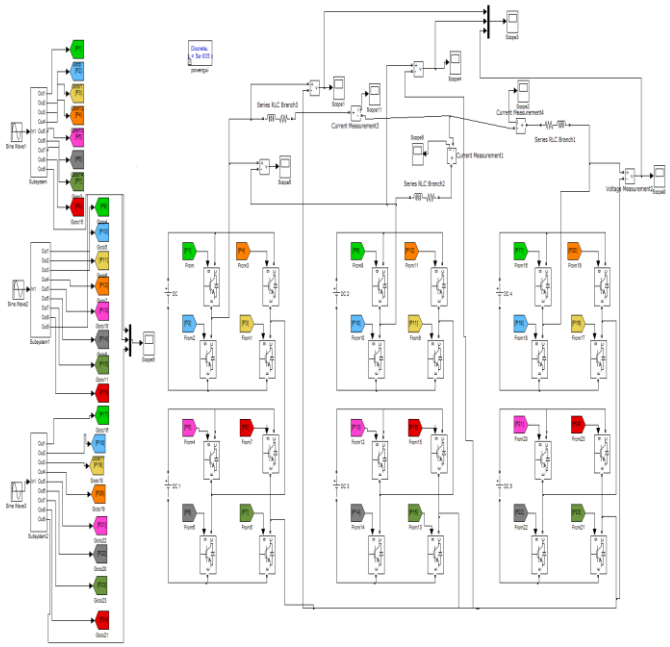

Fig.8.Simulink model of a single phase 5-level CHB-MLI.

To verify that the proposed inverters can be implemented simulations were performed by using MATLAB/SIMULINK as shown in Fig.6, 7, 8. It also helps to confirm the PWM switching strategy [5]. The parameters are chosen as under:

DC voltage ($V_{dc}$) = 100 V
Modulation index ($M_a$) = 0.8
Switching frequency ($f_{cr}$) = 5 kHz
Load: R=10 ohms, L=5 mH [1]

Fig.5. shows the SPWM switching strategy used in this paper. It consists of one reference signal and four triangular carrier signals per phase which produce the gate signals for the switches. The three phase 5-level output voltage (line to line) waveforms of DCMLI, FCMLI and CHB-MLI and the total harmonic distortion (THD) are as shown in Fig.9,10,11,12,13 and 14 respectively. The 5-level voltage helps to reduce the output filters [9].

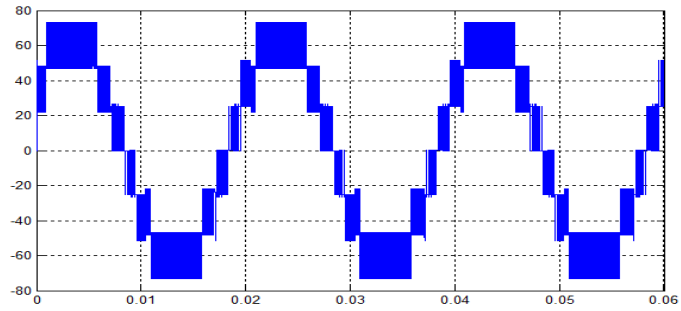


Fig.9. Line voltage of a five level DC-MLI.

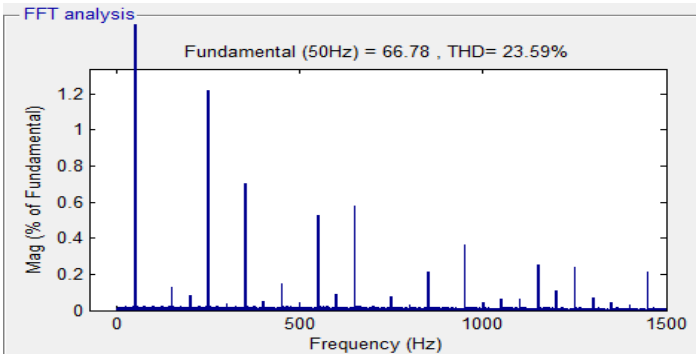


Fig.10. FFT analysis of line voltage of a five level DC-MLI.

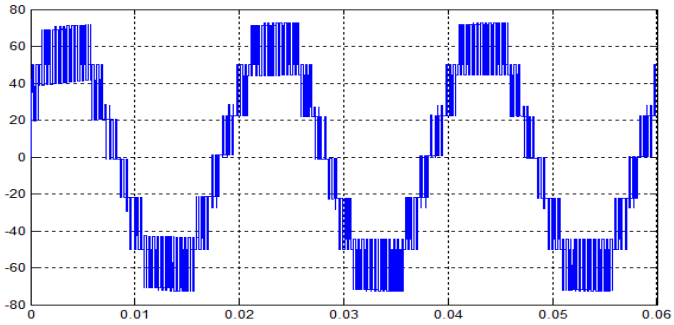


Fig.11. line voltage of a five level FC-MLI.

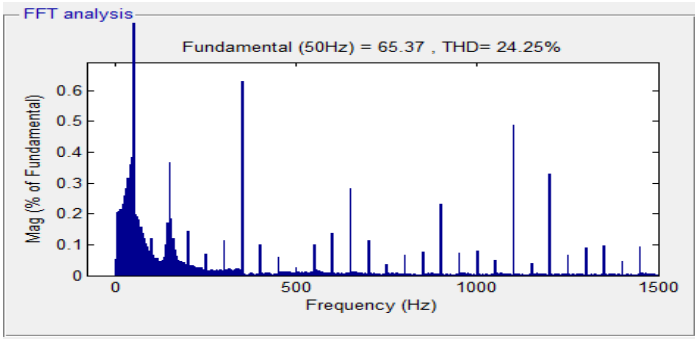


Fig.12. FFT analysis of line voltage of a five level FC-MLI.

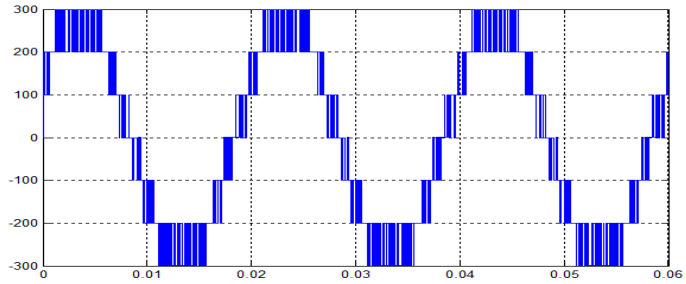


Fig.13. line voltage of a five level CHB-MLI.

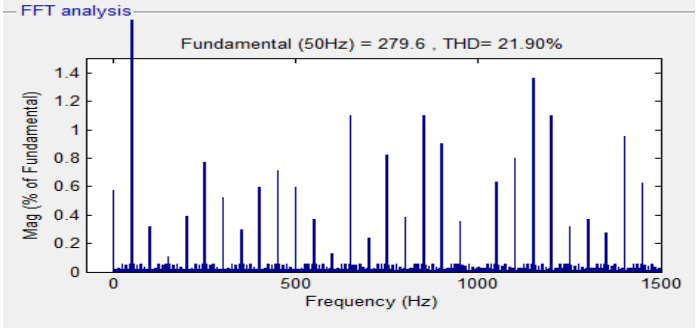


Fig.14. FFT analysis of line voltage of a five level CHB-MLI.

The five level topology of the DC-MLI, FC-MLI and CHB-MLI, has been simulated and the results have been analyzed to get the %THD of the output waveforms. A criterion of comparison is based on the quality of the output voltages (%THD) [10]. In order to get THD level of the waveform, a Fast Fourier Transform (FFT) is applied to obtain the spectrum of the output voltage [2]. The %THD analysis of the line to line voltage waveforms are tabulated in the table I given below. It was observed that the harmonic distortion is less in the CHB-MLI as compared to the remaining two topologies.

TABLE I

| Sr. no. | Topology | %THD |
|---|---|---|
| | | Voltage(line to line) |
| 1. | DC-MLI | 23.59% |
| 2. | FC-MLI | 24.25% |
| 3. | CHB-MLI | 21.9% |

## V. Conclusion

This paper presented three phase Cascaded H-bridge multilevel inverter topology and its comparison with the DC-MLI and FC-MLI. The three phase five level inverters have been modeled and the output have been obtained in MATLAB/SIMULINK. The inverters have been modulated by using the SPWM technique. The analysis shows that the CHB topology has the least number of harmonics in the output voltage.

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