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Design of Area Efficient Low Power CMOS Adder Cell

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Abstract: ***In this paper, by combining XOR/XNOR-based logic and pass-transistor logic with conventional PMOS/NMOS network, a new structure of full adder has been proposed. The evolution of the proposed adder cell from Low Power (LP) XOR/XNOR based SUM to Gate Diffusion Input (GDI) XOR/XNOR based SUM and CARRY with reduced transistor count have been described. Comparisons between the proposed full adder with adders designed by other existing logic styles and their counterparts have been done. The proposed adder outperforms the other full adders, particularly in terms of power consumption, power delay product (PDP) and area.***

Index Terms-
Arithmetic Circuits, CMOS, Complementary pass-transistor logic, **Double pass-transistor logic, Full adder, Gate Diffusion Input, Low-power**

I. INTRODUCTION

Low energy consumption is one of the most desirable properties of modern portable electronic devices. On one side, the high demand of portable electronic devices requires the availability of low power modules for the design of long-lasting battery operated system. On the other side, it requires to design very high speed modules to cope with modern high performance processing applications. The challenge that has been faced by VLSI designers is to find effective techniques and their efficient applications to get minimum power dissipation without any compromise on other performance evaluation parameters. Thus, the design of low power circuits with improved performance is a major concern of modern VLSI designs. In the design of low power circuits, the selection of a proper logic style plays an important role. The combination of certain logic styles and low power modules with low leakage circuit topologies may greatly reduce the limitations of deep-sub-micro-meter technologies.At the system level, in synchronous implementation of microprocessors, adder cells are the basic modules in a variety of arithmetic units such as arithmetic logical units (ALUs), ripple carry adders (RCAs), multipliers etc. Adder cells lie in critical path of these arithmetic units. As the overall performance of a synchronous system depends upon the critical path, a lot of work [1]-[11] has been done dedicated to the improvement of these basic modules and arithmetic structures. The performance of an adder can be significantly improved by efficient implementation of *CARRY* propagation chain. This can be done by improving the structure of 1-bit full adder cell which is the basic building block of adders like carry select or carry skip adders (CSAs) and RCAs. One may also get better performance by employing improved fast adder architectures like carry look ahead and conditional sum adders. Several number of full adders have been designed by academic and research Institutions. The commonly evaluated performance parameters are speed, power dissipation and area. However, with the growth of mobile and embedded applications, power consumption has been given the first priority with regard to circuit and system performance evaluations. Next, the speed improvement and reduction of transistor count has been the aim of many adder designs.

Power consumption mainly consists of static and dynamic power consumptions. Unnecessary switching activity in transistors causes dynamic power dissipation whereas, sub-threshold leakage is the main component of static power dissipation. The delay time varies with the size of transistor, the transistor count per stack, parasitic capacitance and intrinsic capacitance including the capacitive effect of intra-cell and inter-cell routing and the logic depth. The term power delay product (PDP) shows the energy required by the circuit to perform the logical task and it is considered as the better performance parameter for the evaluation of various circuit topologies. Further, the module area depends upon the size of a transistor, number of transistors and routing complexity.

II. EXISTING OPTIMIZATION WORKS

A large amount of work has been done concerning the optimization of low power full adders. These works include standard CMOS adder [1], differential cascode voltage switch (DCVS) adder [2], complementary pass-transistor logic (CPL) adder [3], double pass-transistor logic (DPL) [4], [5], swing restored CPL (SR-CPL) [6], [7], and hybrid logic styles [3], [6]-[8]. Each logic style has been developed with certain advantages and disadvantages over the other existing logic styles.

III. PROPOSED WORK

It has been shown in [9] that some of the full adders exhibit good performance as a 1-bit cell but when employed in complex structures they may show performance degradation. In transmission gate and dual pass transistor logics, both nMOS and pMOS transistors are used in parallel which provide full swing at the output but they have comparatively large number of internal nodes. Ref. [8] shows that wiring complexity of a circuit increases with the increase of internal nodes which further results in high parasitic capacitance and consequently, power dissipation increases.

The proposed adder cell has comparatively less number of internal nodes and hence, low wiring complexity resulting in overall better performance in terms of power consumption and area. In this work, the full adder cell is divided into two parts as shown in Fig. 1 and then further division of these two blocks has

done as per the requirement of power delay and area reduction. By dividing the adder cell into separate *SUM* and *CARRY* blocks certain advantages have been achieved. Primarily, it facilitates separate tuning of propagation delay of *SUM* and *CARRY* outputs. Secondly, the input capacitance of the circuit has been reduced as the inputs to most of the transistors have been applied at the gates instead of some drain or source terminals.

For the implementation of proposed adder cell (see Fig. 1), the following logical equations are used. The equations for the XOR, XNOR and Multiplexer in *SUM* circuit of the proposed adder are shown below:

$$SUM = X.C_0 + \overline{X}.C_1 \quad (1)$$

$$X = A \otimes B \quad (2)$$

$$\overline{X} = \overline{A \otimes B} \quad (3)$$

The equations for the pMOS and nMOS networks in *CARRY* circuit are expressed as:

$$C\_P = \overline{A}.\overline{C_{in}} + \overline{B}.\overline{C_{in}} + \overline{A}.\overline{B} \quad (4)$$

$$C\_N = \overline{A}.\overline{C_{in}} + \overline{B}.\overline{C_{in}} + \overline{A}.\overline{B} \quad (5)$$

In the implementation of the proposed adder cell, low power (LP) XOR and low power (LP) XNOR [10] have used for implementation of XOR and XNOR blocks of adder cell, multiplexer has implemented using DPL logic [4], *CARRY* circuit has been realized using pMOS and nMOS networks [11]. The resultant proposed adder has simulated and compared its performance with the existing adder cells [8] and it was found that it consumes less power but at the cost of increased transistor count.

Next, both *SUM* and *CARRY* circuits have worked out to

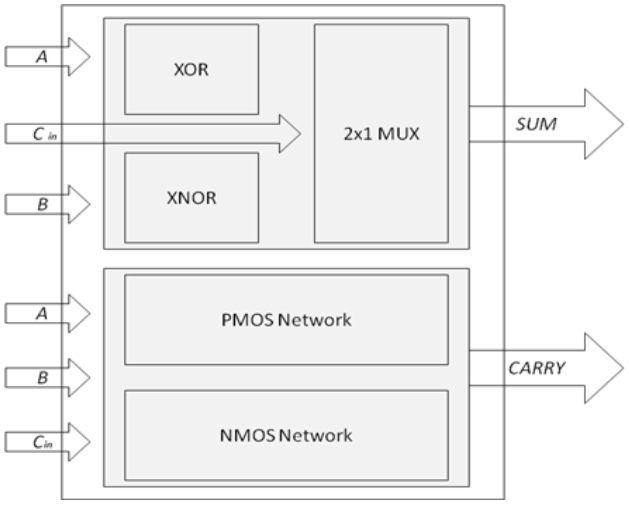
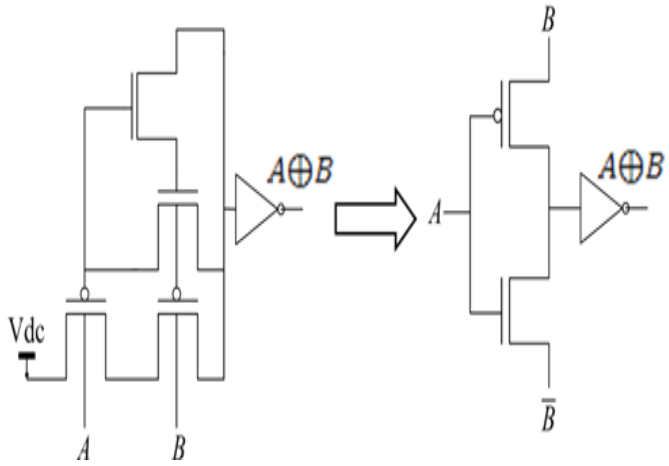
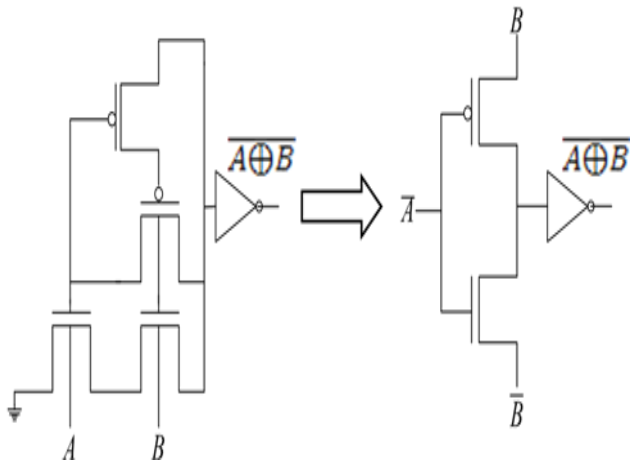


Fig. 1 Block diagram of a full adder cell with different sections



(a)



(b)

Fig. 2 Replacement of (a) LP XOR by GDI XOR and (b) LP XNOR by GDI XNOR

get an adder cell with reduced power dissipation and less transistor count. For this, as shown in Fig. 2, the LP XOR and LP XNOR in the *SUM* circuit have replaced by gate diffusion input (GDI) based XOR and XNOR [12], respectively. In general, it has been observed that inverters used after GDI XOR and GDI XNOR are for the purpose of logic level restoration. In this work, the two inverters after GDI XOR and GDI XNOR of the *SUM* circuit have replaced by a single inverter after multiplexer (see Fig. 3). By doing so, inverted sum has obtained at the output. In order to get the true logic, the position of XOR and XNOR logics has interchanged.

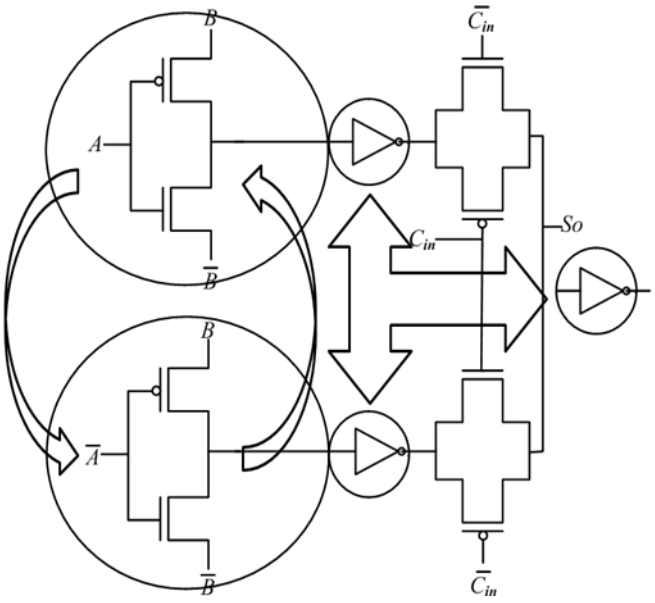


Fig. 3 Adjustment in *SUM* circuit to reduce transistor count

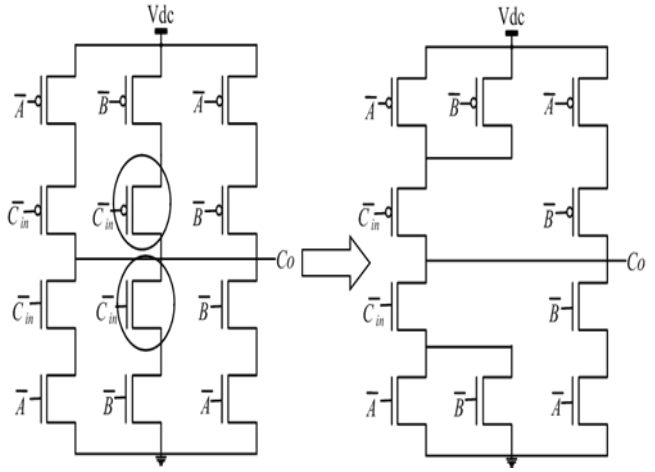


Fig. 4 Reduction of transistor count in *CARRY* circuit

Under the same course of work, it has also been observed that in the pMOS and nMOS networks of *CARRY* circuit, the two transistors with common input (C_{in}) pass the same signals at different input conditions. In view of this, as depicted in Fig. 4, these two transistors have replaced by a single transistor. Now, the logic equations of the *CARRY* circuit are reduced to:

$$C\_P = \overline{C_{in}}.(\overline{A}+\overline{B}) + \overline{A}\overline{B} \quad (6)$$

$$C\_N = \overline{C_{in}}.(\overline{A}+\overline{B}) + \overline{A}\overline{B} \quad (7)$$

for pMOS and nMOS networks, respectively. Finally, an adder cell with the proposed topology is shown in Fig. 5. The layout of proposed adder cell with minimum area as compared to other adder cells is shown in Fig. 7.

IV. SIMULATION SETUP

Fig. 6 shows the test bed set up for comparison of full-adders cells [5], [8] and [9]. The size of input buffers induces some degradation in the input signals and size of

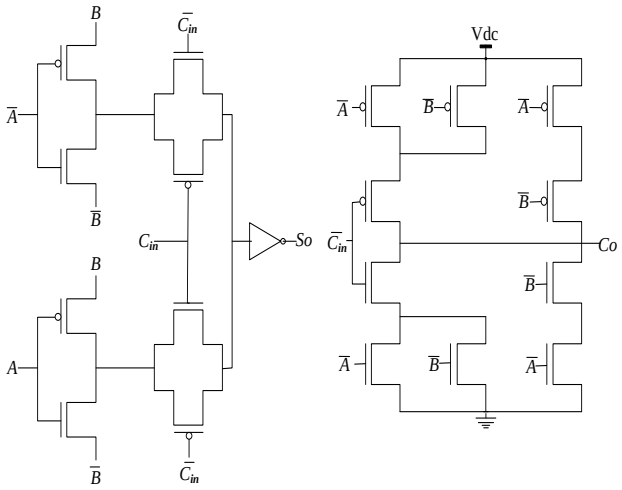


Fig. 5 Proposed adder cell

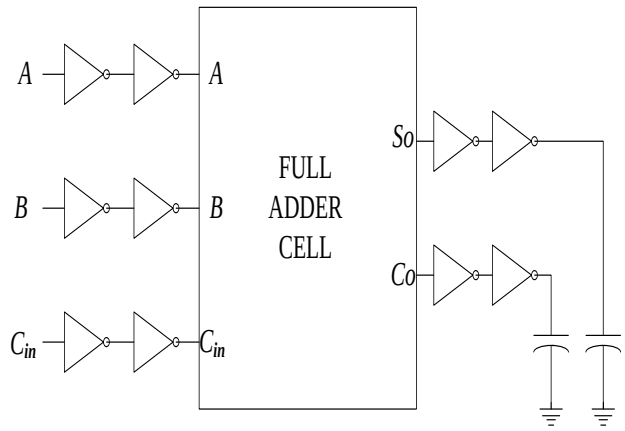


Fig. 6 Test bed set up for simulation of full adder cells

output buffers provides load equivalent to four small inverters letting the full adder cell experiences as if it has been used as a part of some larger circuit. This set up includes the short circuit consumption of inverters connected to the inputs. The effects and power consumption of the static inverters at the inputs and outputs provide a good generalization for any operating scenario to be considered because Devices Under Test (DUT) are going to be used with other devices as a part of larger system.

V. SIMULATION RESULTS

In this work, the comparison of various full-adders, namely, HPSC [7], Hybrid [3], Hybrid CMOS [8], CPL [13], DPL [5] and SR-CPL [5] has done. The schematics and layouts have designed using UMC 0.18-µm CMOS technology and simulated

using the BSIM3v3 model (level 49). Simulations have carried out using HSPICE [14] to measure the power consumption and propagation delay of the full adders.

Table I shows the comparison of various full adder cells in terms of power consumption, propagation delay, PDP and area. These full adder cells have given the same input conditions of 1.8 V supply and the maximum frequency of 200 MHz. Results for the whole test bed (*t-bed*) and for the full-adder alone (*fa*) have shown in Table I.

TABLE I
COMPARISON OF VARIOUS FULL ADDER CELLS

Adder design		**Avg. power (µW)**	***%fa/ t-bed***	***Delay* (ps)**	***PDP* (fj)**	**AREA (μm^2)**	**F_{max} (GHz)**	***VDD_{min}* (V)**
HPSC	*t-bed*	483.02	70.06	259.9	87.95	410	0.25	1.2
	fa	338.41						
HYBRID	*t-bed*	452.50	63.95	157.67	45.61	447	0.80	0.7
	fa	289.38						
Hybrid CMOS	*t-bed*	413.21	66.81	184.92	50.99	421	0.80	0.8
	fa	276.07						
CPL	*t-bed*	403.35	41.07	192.67	31.93	372	1.50	0.6
	fa	165.74						
DPL [8]	*t-bed*	279.22	35.58	80.52	8.04	238	1.25	0.6
	fa	99.35						
SR CPL [8]	*t-bed*	291.41	41.91	78.93	9.64	235	1.25	0.6
	fa	122.13						
Proposed Adder cell	*t-bed*	203.77	31.78	85.79	5.46	136	1.25	0.6
	fa	64.78						

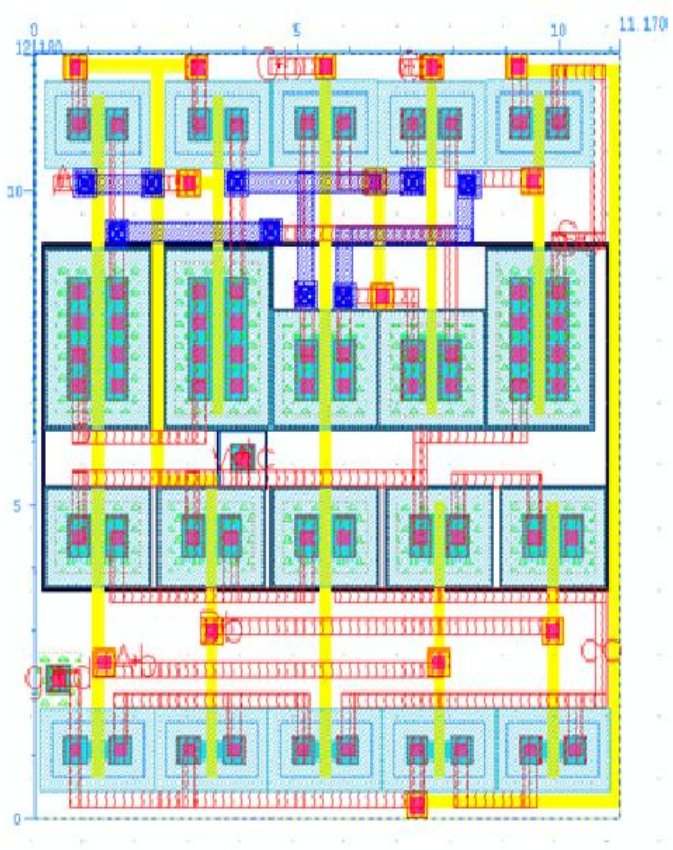


Fig.7 Layout of proposed adder cell

Terms used for comparison of adders:

- *Adder design*: It represents the full adder cell with different logic styles and separates the result for the whole test-bed (*t-bed*) and the adder cell alone.
- *Avg. Power*: It indicates the average power taken from the power supply and the module inputs (eg. some adders use energy of the inverters at the inputs).
- *% fa/t-bed*: It represens the percentage of power consumed by the full adder cell under test with respect to the power (to that) consumed by the whole test bed.
- *Delay*: It refers to the longest propagation delay for the *SUM* and *CARRY* output signals with respect to input signals.
- *PDP*: It is the product of power and delay showing the performance of the cell in terms of power consumption
- and propagation delay. It represents the overall performance that can be matched in a better way by balancing these two separately.
- VDD_{min}: It is the minimum supply voltage that is essential for the correct functionality of the full adder cell so that it can drive output buffers and maintain proper logic values at the outputs.

VI. CONCLUSIONS

In this paper, a new full adder cell has been proposed with reduced power consumption and area. The adder cell has been presented with low power XOR/XNOR based *SUM* and conventional NMOS and PMOS networks based *CARRY* circuits. Optimization has been carried out to further reduce the have shown that this full adder achieves a better PDP and area when compared with the existing ones. By analyzing these results, one can say that in other designs, such as RCA and total power consumption and area. The cost is a small increase in delay due to addition of inverter for level restoration in *SUM* part of circuit. Simulations in deep-sub-micro-meter technology multipliers, the intrinsic benefits of this new adder could be more fully exploited.

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