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Minimization of IR Drop Using Diagonal Power Routing Technique in Nanometer Era in VLSI

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Abstract:One of the new technique which is notable for dealing problems such as high frequency effect due to inductance and capacitance in physical layout level other than existing of techniques. For most designs for the use of 45nm processing technology the analysis using a static approach is no longer sufficient and it becomes mandatory to analyse the actual variation of the supply voltage with respect to time for detecting chip failure conditions.In this paper we deal with the IR drop analysis of the Diagonal power grid and orthogonal power grid, comparison between the diagonal and orthogonal power grid. Full chip Diagonal power grid static and dynamic IR drop analysis optimization of power in vlsi digital design using red hawk for nanometer era

1.Introduction

With the advanced technology one of the main challenges facing the chip designers is signal Integrity, IR drop and Electro Migration. With increasing operating frequencies and elevating power consumptions in VLSI circuits, the design and analysis of on chip power distribution networks has become a critical design task. The definition of the Signal integrity is the ability of the performance of the signal without any distortion in a circuit . if signal integrity is occurs then that will be exhibits malfunctioning of the circuit [1]. Which deals with voltage variations and delays of transition when it is in active mode .various interference of signal problems have been studied for nanometre era .In which most emphasizing on cross talk and variations of supply voltages V_{DD} and ground V_{SS} [2,3] and for high frequency effects like antenna and transmission line effects [4,5],about the power supply noise and signal skew [6,7,8,9] signal propagation delay [10,11]also have been studied .we focused mainly on the aggressive interconnect scaling has increased the average current density and the resistance per unit length of wires and on-chip Inductance. Since the supply voltage level is also reduced with the technology scaling, the power supply noise becomes even more pronounced because the ratio of the peak noise voltage to the ideal supply voltage level increases with each scaled technology node. The power supply noise mainly manifests itself as a voltage drop in the power distribution networks.

Local and Global IR drop

IR drop and ground bounce can be both local andglobal phenomena. They can be local phenomena when a number of cells in close proximity switch simultaneously, causing IR drop or ground bounce in that localized area. A higher power grid resistance to a specific portion of the chip can also cause localized IR drop or ground bounce. They can be global phenomena when activity in one region of a chip causes effects in other regions. In an ideal powergrid with equally distributed current and peripheralpower pads, the power grid has a set of equipotentsurfaces that form concentric circles centered in themiddle of the chip as The center ofthese concentric circles has the largest IR drop or ground bounce, and the amount of the effectdecreases toward the pads; its continuities in thesecircles typically identify regions containingdiscontinuities in the power grid or unequallydistributed current flow. Large amounts of IR drop orground bounce can be caused by simultaneousswitching of cells and transistors. If all cells andtransistors of a design switched at once, the local orglobal IR drop or ground bounce on a chip would beextremely large.Potential causes of simultaneousswitching are the following:a) Synchronized clock networks b) Bus drivers c) Memory word line drivers d) Signal I/O circuitry e) Any groups of large drivers designed to switch together

2 . Pin and Grid based Abstraction

In grid-based modeling, the memories are considered with their internal power grids. The current draw is distributed among the power pins of the block that connect to the top level grid. This method of modeling is particularly useful in designs for which full-chip power grid connectivity is maintained through the power grid of the memory block(s). For example, if the top-level power grid of a design is in metal layers 3 and 4, and the memory blocks have power grids in metal layers 3 and 4, then the inclusion of the memory blocks along with their power grids will ensure connectivity for the power routes in metal layers 3 and 4. If these memory blocks were black-boxed, then the continuity and connectivity of the power routes in these layers would be lost. Figures 1 and 2 illustrates this situation.

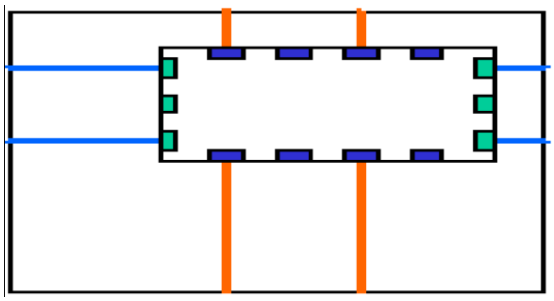

Figure1 Black boxed modeling Loss in connectivity in top level power gird

However, in this grid-based modeling framework, the current draw is considered at the pins of the memory block. So it is useful when faster run-times are required or when memory capacity is an issue. Considering the current demand inside the memory down to the lower levels of metals, as opposed to at the pins, adds significant overhead in computation time and physical memory usage. But this method has the advantage over the

black-boxed modeling in that it considers the memory power grid during analysis.

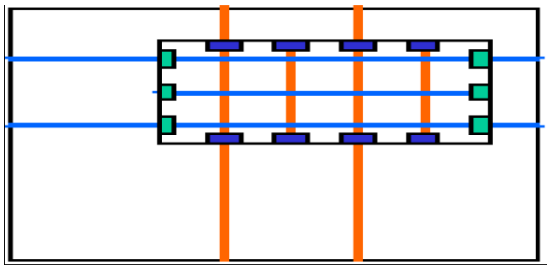

Figure2 Pin and Grid based modeling Continuity in top level grid preserved from the inclusion of block level PG network.

Detailed Modeling

In detailed modeling, the power grid of a memory block is extracted and current sources, along with decoupling capacitances, are placed at appropriate locations inside the memory. This allows for an accurate consideration of current flow inside the memory blocks. It also allows for modeling of a memory's dynamic switching effect on its surrounding logic.
The final step in the designed flow is Dynamic Power Analysis part. Here we analyze the results obtained from the run. We later perform what if analysis to overcome problems if there are any. The results are attached in the coming pages along with the problems faced.

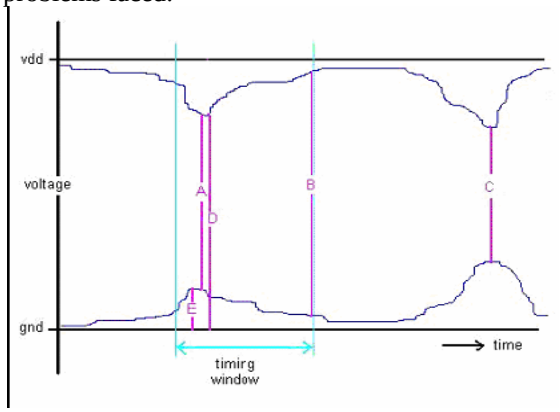

Fig3 Showing Voltage Drop and Ground Bounce

Where
A: Minimum_Vdd-Vss_over_a_TimingWindow
B: Maximum_Vdd-Vss_over_a_TimingWindow
C: Minimum_Vdd-Vss_in_a_Simulation
D: Minimum_Vdd
E: Maximum_Vss

3.Flow setting of the power grid analysis

When we analyze the IR drop analysis with Redhawk we required to mention the some of the parameters which is related to the design. The main parameters such as Frequency of the design, Library, Temperature, Functional corner, which spef's, operating voltage, data toggle rate, RAMS libs and standard cell libs.

In our design, we consider that the bellow is the operating condition parameters Frequency = 940 MHz , Library = tt0p9v110C,Temp = 110C, TW = FuncTT , Spefs: typrc110 Voltage: 0.90v, Activity Factor = 0.125,RAMS = lib_3.0.7, StdCells = lib_3.0.7,Design corners for APL (apache power library)
IR = tt0p9v110c_0.9V_110C,
EM = ff0p99v0c_0.99V_110C

4. Diagonal power grid IR Drop analysis

In this the top power grid metals are M9 and M8 which are the RDL layers. Metal M9 is routed diagonally with 45 degrees and M8 is routed horizontally. In present technology power consumption of the design is more. The problem is with the power delivery system. The IR drop is proportional to the average current consumed by the circuit in the chip. The L.di/dt drop is proportional to the time-domain change of the current due to the switching of the logic gates in the chip operation. The diagonal (M9) power grid is reducing the resistance and L di/dt effects. In this design M9 is routed with the 45 degrees to the M8 metal, in this case the no of vias between the M9 and M8 is increases and the effective resistance is less in the chip level. The power supply is connected from the M9 to the follow pins, in tile (block level) M7 is vertical power mesh and M6 is discontinued power mesh. In this analysis we considered the 4 blocks information in tile level and remaining blocks are block boxes, because of the run time and disk space, even we considered same information in orthogonal power grid for the comparison purpose.
The below table 1 shows the IR drop voltage information of the blocks in regions in the blocks. It will give the worst voltage drop information

Table 1 Diagonal IR drop information of the blocks

Block name	IR Drop (mv)	Ir drop (%)	% inst ≥13 %	%inst ≥12%	%inst ≥10 %	No inst≥ 13	No inst ≥12 %	No Inst ≥10 %
x1	140.00	15.56	0.09	5.75	46.34	146	9374	75552
x2	131.50	14.61	0.01	0.57	10.68	9	460	8616
x3	113.20	12.58	0.00	0.11	12.57	0	298	33956

In the above table listed three designs **x1**, **x2** and **x3**. The maximum IR drop in the design x1 is 140mv. The design supply voltage is 0.9v. This drop is the 15.56% of the supply voltage. The drop in the design we divide into the range like the percentage of the instances in the design greater than the divide range which is easy to study in the respective range according to requirement. The design x1 having the %of instances is greater than 13% is 0.09%, similarly greater than 12 and 10% as shown in table. The no if instances in the design x1 are greater than 13% is 146, table gives detail information for different range.

In the design x2 the maximum IR drop is 131.5mv, the Red hawk tool will analyze the IR drop is cell based this will indicate the worst IR drop at cell node. In the x2 design the maximum drop is 14.6%. The table shows the percentage instances and number instances.

The design x3 has a maximum voltage drop 113.20mv and 12.58% in the supply voltage. The percentage of instances greater than 13% is 0, this block contain the less IR drop compare to the other blocks.

The contour map of the IR drop of the diagonal power grid design as shown in below fig 4

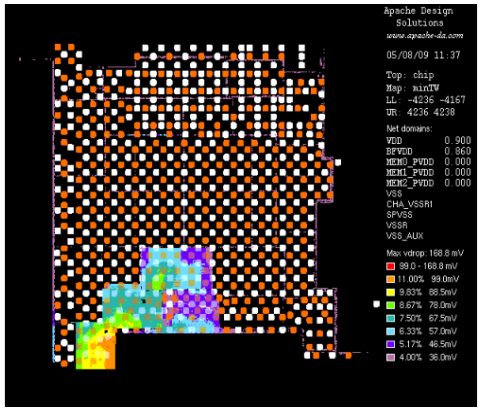

Figure 4 shows the IR drop of the Diagonal power grid design

The red hawk will give the map of the voltage drop in the design with the different colors. The color range can be changed in the red hawk by user requirement. In the above map the red color is shows the IR drop greater than 12%. Similarly we can set the different colors for different range generally red will for high IR drop.

The Diagonal power grid design have very less red spots in the design, with the help of map we can directly go to that particular region easy to identify the what is the cause of more IR drop.

4. Orthogonal Power Grid IR Drop analysis

In this the top RDL layers are M9 and M8. In this case chip level the power grid M9 and M8 are orthogonal to each other. The Layer M9 is routed vertically and M8 is horizontally. In block level M7 is the power mesh and M6 is power mesh with discontinues. The bottom layers are stacked vias up to the follow pin.

The no of vias between the M9 and M8 is less compared to the Diagonal power grid , the resistance is more and also the length of the layers are more compared to the diagonal.The table 2 shows the IR drop information of the different blocks.

In the Orthogonal power grid analysis same block as considered to the diagonal power grid. The top layer routing is different. The diagonal power grid analysis the design x1 has the maximum voltage is 148.40mv and the percentage of voltage drop is 16.49mv from the supply voltage. The instance percentage greater than 13% is 0.51% and the number instances are 832.The design x2 has the 137.43mv maximum IR drop which is the 15.27% in the supply voltage. The percentage instances greater than 13% is 0.02%. The design x3 has the maximum of 119.16mv and 13.24% of the supply voltage.The table indicates the information about the three blocks of the maximum voltage drop and corresponding design percentage instances.

Table 2 Orthogonal power grid IR drop Information

	IRDrop(mv)	IRdrop (%)	%inst >=13	%Inst >=12	%Inst >=10	Nr inst >=13 %	Nr Inst >=12 %	Nr Inst >=10 %
x1	148.40	16.49	0.51	7.67	49.74	832	12509	81095
x2	137.43	15.27	0.02	0.04	11.58	18	840	9343
x3	119.16	13.24	0.01	2.31	14.96	27	6240	40412

5 Comparison between the Diagonal and Orthogonal power grid

The above information gave the IR drop results with different grid structure. In the diagonal power grid the IR drop is less compare to the orthogonal because of the resistance and L.di/dt effects, the less resistance is due to the more parallel vias in diagonal compare to the orthogonal. In the Diagonal grid the current loop path is less compared the orthogonal due to this the L.di/dt effect is less.

In above cases the design x1 has 8mv less IR drop in the diagonal compared to the orthogonal and also the percentage and the number of instance is come down from higher voltage drop to lower drop region. The design x2 benefited the 6mv compared to the orthogonal power grid. The number instances greater than 10%is come down from 9343 to 8616.

Similarly the design x3 also has 6mv less compare to the orthogonal power grid. The overall from the 3 design an average 6 to 8mv is less in the diagonal grid. In the IR drop maps also the red areas is more in orthogonal power grid compared to the Diagonal. From the above analysis we implemented the diagonal power grid in chip level power grid to reduce the IR drop problems.

6. Dynamic IR drop Reports

The below are the dynamic voltage drop block wise details

Redhawk will analyze the V_{SS}, V_{DD} together and separately, we need to make sure that there is no short between the V_{SS} and V_{DD}.The redhawk will also give the contour maps of the drops as shown in below this map is combination of both V_{SS} and V_{DD} drop together. As shown in fig 5

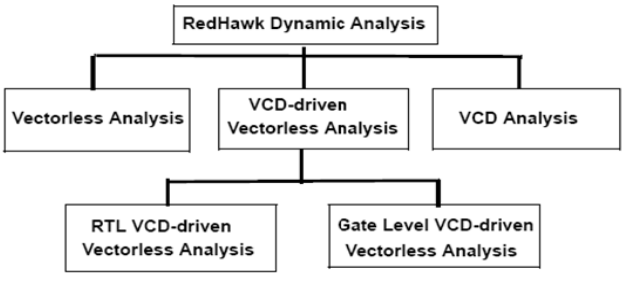

Figure 5 Types of Redhawk Dynamic Analysis

In the above fig the worst drops are at the outer region, in the flip chip design the signal and power connection are through the bumps. In the design where the power bump pitch is more in that region the drop is more ,the pitch is more in some regions because of the in between the power bumps the signal bumps are present. In the fig the regions with red color shows the more IR drop compared to the other regions

Table 3 dynamic IR drop using redhawk reports

Tile	IR drop(mv)	% of IR
Core/zzz_00	280.3	31.1444
Core/zzz_01	284.4	31.6000
Core/zzz_02	262.7	29.1889
Core/zzz_03	198.5	22.0556
Core/zzz_04	304.6	33.8444
Core/zzz_05	123.7	13.7444
Core/zzz_06	515.9	57.3222
Core/zzz_07	205.1	22.7889
Core/zzz_08	254.6	28.2889
Core/zzz_09	177.7	19.7444
Core/zzz_10	250.2	27.8000
Core/zzz_11	209.3	23.2556
Core/zzz_12	258.2	28.6889
Core/zzz_13	209.7	23.3000
Core/zzz_14	213.7	23.7444
Core/zzz_15	226.6	25.1778
Core/zzz_16	216	24.0000
Core/zzz_17	413.5	45.9444
Core/zzz_18	93.5	10.3889
Core/zzz_19	191.8	21.3111
Core/zzz_20	73	8.11111
Core/zzz_21	246.1	27.3444
Core/zzz_22	179.9	19.9889
Core/zzz_23	370.1	41.1222
Core/zzz_24	144.9	16.1000
Core/zzz_25	369.7	41.0778
Core/zzz_26	199.6	22.1778
Core/zzz_27	382	42.4444
Core/zzz_28	188.3	20.9222
Core/zzz_29	370.3	41.1444

Table 4 various parameters in the process of ir drop for different cells

Cell_type	Total_pwr	Leakage_pwr	Internal_pwr	Switching_pwr	%total_pwr
Combinational	1.8396e+01	1.6648e+00	6.1896e+00	1.0541e+01	4.0642e+01
Latch_and_FF	1.6516e+01	1.0029e+00	1.3759e+01	1.7544e+00	3.6491e+01
Memory	7.9349e+00	6.4625e-01	4.4691e+00	2.8196e+00	1.7531e+01
Clocked_inst	2.3755e+00	4.6938e-02	1.4854e+00	8.4314e-01	5.2482e+00
Decap	3.9921e-02	3.9921e-02	0.0000e+00	0.0000e+00	8.8199e-02

7. Power summary of the design

The redhawk will calculate the power of the design during analysis by performing power calculation. As shown in below

Power of different frequency (MHz) domain in Watt: Power of different Vdd domain in Watt: Vdd_domain total_pwr leakage_pwr Internal_pwr switching_pwr %_total_pwr

VDD (0.9V) 4.4755e+01 3.3513e+00 2.5601e+01 1.5803e+01 9.8879e+01

Power of different cell types in Watt:

Total chip power, 45.262 Watt including core power and other domain power.

Total clock network only power, 7.0583 Watt. Total clock power including clock network and FF/latch clock pin power, 20.905 Watt.

In above report indicating the power consumption design for at all frequencies if the design have one more. It categorize the total power consumption at part particular frequency and from that what is leakage power , internal power and switching power ,percentage of the total consumption of the chip.

In this at 940 MHz total power is 40.18 watts, which is 88.77% of the total power remaining power is consumed by other frequency.

It will also reports the power consumption of the different voltage domains, the blocks in the design's operated in two voltage modes one is 0.9v and another is art 1.1v, in this we not reporting the 1.1v ,in design we have only one sub blocks operated at 1.1v. The redhawk will also report the power consumption of the each cell , as shown in above it will reporting the all combinational cell, latches and flip-flops ,memories, clock cells and decaps separately.

8.**Conclusion** : In this we implemented the Diagonal power routing in top power layer (M9), which reduce the resistance and Inductance (Ldi/dt) effect compared to the orthogonal power grid. This is used to overcome the problem identified which in the view of voltage drop reduces due to the setting of 8&9 metal layers at the stage of physical layout design .this technique have good performance over existing one .by using of this technique to minimize the IR drop in physical design ,which leads that this technique is very much useful at the physical design for reducing the cost as well as the prediction of functionalities of a model.

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