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Transient Analysis of Second-Order Charge Pump PLL for Phase Step Input

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Abstract: This paper presents the analysis and simulation of second-order charge pump phase-locked loop by applying the phase step at the entrance and calculates the fast lock and transient time and the effects of loop parameters such as capacitor, resistor, loo filter current, control voltage oscillator at the at the fast lock investigated and plotted in the diagram at transition time. All simulation was performed by matlab software.

Keywords: Phase Locked Loop (PLL), Charge Pump (CP), Phase Detector (PD), Settling time(t_S), Damping ratio (ζ), Overshoot, Peak time, Rise time(t_r).

I. Introduction

The phase-locked loop is a component which has been used widely in various fields of integrated circuits at the recent years generally, have been used as a VLSI timer production or frequency divider of communication systems [1]–[6]. Fast locking is a key performance for the ranking of frequency divider, especially in wireless applications where the speed of frequency divider shows that the communication how fast that can be switching between one channels to another or switching between off position to on position. The phase locked loops (PLL) are used widely foe timer, synchronization and frequency combinations [7], [8]. Reduce of a PLL lock time is common place by using the dynamic loop bandwidth. Must consider two mechanisms for conventional PLL. Which one of this is learning frequency and another is learning phase. During the frequency learning a convention phase/frequency detector (PFD) may have cycle slip problem which increases the lock time of PLL. However a frequency learning of PLL is completed, redistributions occur in a disable second-order loop filter when a charge pump (CP) is off. Which lead to the residual phase error and increase the time of the PLL meeting [9]–[11]. The main tasks of the phase-locked loop are producing the clock in microprocessors, and application in receiving system and frequency synthesizer. The main challenges in phase-locked loop can be transient analysis or in other words lock time analysis and reduce it, mentioned persistence and jitter analysis which one of the designer's goals is calculating lock time and effort to reduce it. In this paper, first simulate the second-order charge pump phase-locked loop by applying at the entrance phase step and calculate the fast lock and transient time and plot the transient time diagram and finally consider the effects of loop parameters on fast lock and analysis the simulation results.

II. Second-order charge pump PLL architecture

Figure.1 is shown the second-order phase-locked loop with loop filter [12]–[14]. A second-order charge pump phase-locked loop is include of phase/frequency detector (PFD), a charge pump (CP), a loop filter (LF) and voltage controlled oscillator (VCO). Charge pump includes of two current switches which send the charge pump into or out of the loop filter. In fact, the charge pump in PLL switched by detector and generates positive and negative current which sent the charge pump into or out of the loop filter that cause of charge or discharge of the capacitor to control the VCO in PLL, in other words lead to increase the lock range. Phase or frequency input source (Vin) and the output source (Vout). The output signal compared with PFD and convert to the current on charge pump (Ip). Noise and high frequency at the output of the charge pump removed through the loop filter which contain of Cp and Rp. The output signal of loop filter leads to run VCO and generate a signal with frequency which depends on voltage of control (Vcont). This capacitor is typically much smaller than the capacitor Cp. Figure 2 is shown the PLL structure in phase area. This model is the behavior of simulation at phase area in the system level in order to consider the derived expression. Figure 3 is shown the alternative phase area model which Kvco is the gain and Ip is the charge pump current. The second-order closed-loop transfer function in figure is shown below.

$$G(s)\big|_{open} = \frac{I_P}{2\pi}\left(R_p + \frac{1}{C_p s}\right)\frac{K_{vco}}{s} \tag{1}$$

$$H(s)\big|_{close} = \frac{C(s)}{R(s)} \tag{2}$$

$$= \frac{\frac{I_p K_{VCO}}{2\pi C_p}(R_p C_p S+1)}{S^2 + \frac{I_p K_{VCO}}{2\pi} R_p s + \frac{I_p K_{VCO}}{2\pi C_p}} = \frac{\frac{I_p K_{VCO}}{2\pi C_p}}{S^2 + 2\xi\omega_n s + \omega_n{}^2}(R_p C_p s+1)$$

$$K_V = I_p K_{VCO}/(2\pi C_p) \tag{3}$$

For second-order systems are:

$$\zeta = \frac{R_p}{2}\sqrt{\frac{I_p R_p K_{VCO}}{2\pi}} \tag{4}$$

$$\omega_n = \frac{1}{2} R_p \frac{I_p K_{vco}}{2\pi} = \sqrt{\frac{I_p K_{vco}}{2\pi C_p}} \tag{5}$$

$$\omega_{PM} = \frac{R_P I_P K_{VCO}}{2\pi} \tag{6}$$

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$$\omega_L = \sqrt{1 + 2\xi^2 + \sqrt{2 + 4\xi^2 + 4\xi^4}} \quad (7)$$

$$\omega_H = 2\xi\omega_n = 2\left(\frac{R_P}{2}\sqrt{\frac{I_P R_P K_{VCO}}{2\pi}}\right) \times \left(\sqrt{\frac{I_P K_{VCO}}{2\pi C_P}}\right) \quad (8)$$

$$\angle G(\omega) = -180 + \tan^{-1}(R_P C_P \omega_{PM}) \quad (9)$$

Phase margin in the second-order PLL is given by the following equation:

$$PM = 180 + \angle G(\omega) = \tan^{-1}(R_P C_P \omega_{PM}) \quad (10)$$

For stable system, phase margin is between 60 to 70 degrees and the damping ratio (ξ) is approximately 0.6 to 0.7. If the phase margin was not desirable, Ip must be increase and if these increases lead to ω_H increased excessive, the capacitor Cp must be selected as large as possible.

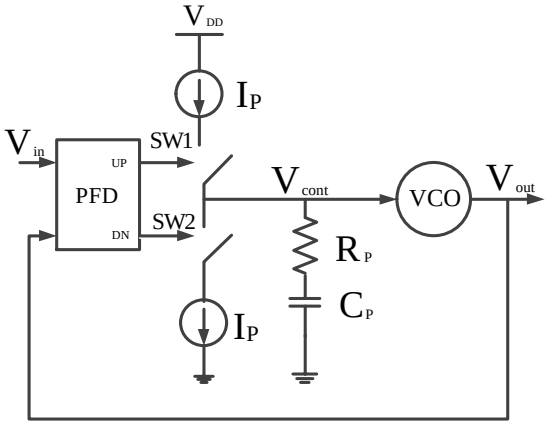

Fig 1.the structure of second order phase lock loop with loop filter

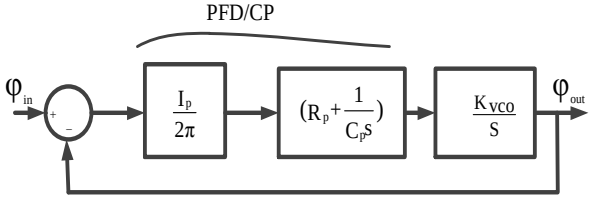

Fig 2. Phase area model of PLL

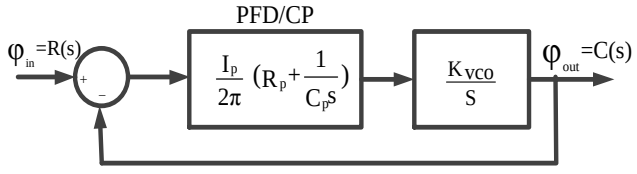

Fig 3. Phase area structure in PLL

III. **The behavior of phase-locked loop by applying step at input**

In this section, the PLL behaviour by applying step input considered and also analysis the behaviour of phase locked loop and calculate the lock time and transient time and plot it on diagram. Unit step response of second-order system is as follows:

$$C(t) = 1 - \left(e^{-\alpha t} / \beta\right) \sin(\omega_d t + \theta) \quad (11)$$

Which α is the damping and ω_d is the natural frequency of self-damping system. Figure 4 is shown the curve of unit step response of a second-order system [15] which includes the following items: 1. the rise time (t_r) 2-maximum overshoot (Mp) 3.setting time (t_s) 4.peak time (t_p).

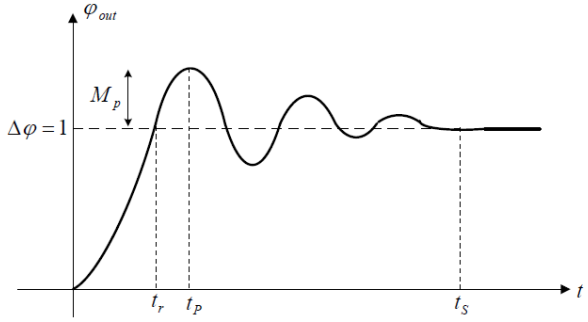

Fig 4.unit step response curve

Now, examine the effect of the phase shift (or charge). By assuming the sinusoidal input is $V_{in} = A\cos(\omega_0 t)$ and the phase of this change suddenly to θ. In this case $\varphi_{in} = \omega_0 t + \theta$. So $d\varphi_{in}/dt = \omega_0$ and by placement in following equation:

$$\frac{dv_{cont}}{dt} + K_{PD}K_{VCO}V_{cont} = K_{PD}\left(\frac{d\varphi_{in}}{dt} - \omega_0\right) \quad (12)$$

By solving the above equation:

$$\frac{dV_{cont}}{dt} + K_{PD}K_{VCO}V_{cont} = 0 \quad (13)$$

The equation is shown if the input frequency is the same with VCO centre frequency and only the initial phase change, after the time, the voltage control Vcont reach to zero and the output frequency reach to ω_0 too and in these conditions we have.

$$\omega_{in} = \omega_{out} = \omega_0 \quad (14)$$

$$V_{cont} = 0 \Rightarrow \varphi_{in} = \varphi_{out} \quad (15)$$

Figure 6 is shown the block structure simulated of second-order phase-locked loop by applying phase step in phase area and in Matlab software. The initial values in phase area are shown in table 1. Figure 7 is shown the output phase of the simulation as you can see, the action of loop lock is done and within a period of time the value of input and output of phase are the same. Now, should try to reduce the amount of overshoot, because reduce the overshoot lead to increase the stability.

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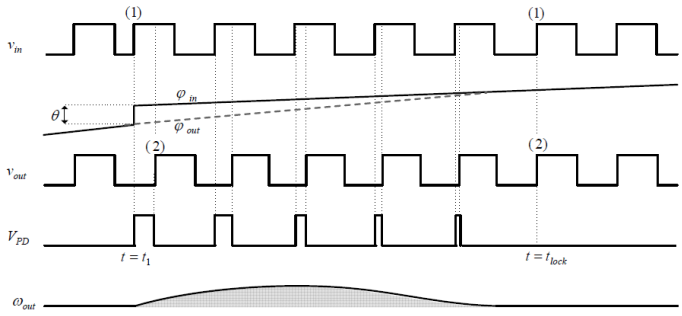

Fig.5. PLL behavior by applying phase step

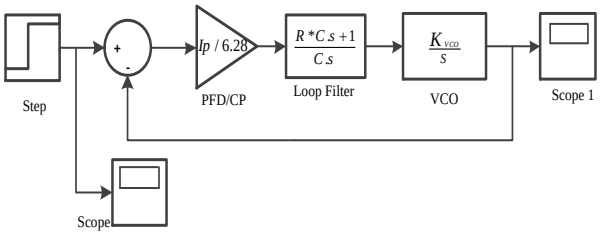

Fig .6.simulated PLL in Matlab software at phase area.

Table 1.the initial values add the phase's area.

C	220pf
R	2.2kΩ
Kvco	130MHz
Ip	100μA

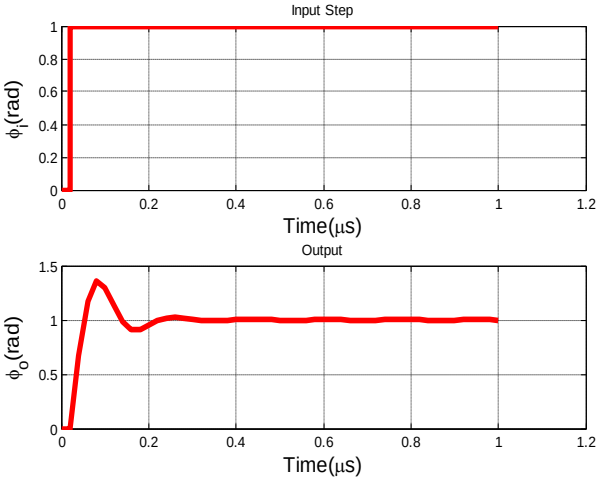

Fig 7.the output simulation by phase step input

If we want the output phase reach to input phase, at the timescales of output frequency which is the slop (derivative) of output phase must change based on the phase difference which PLL simulated at phase area with the slope input in shown at the figure 8.

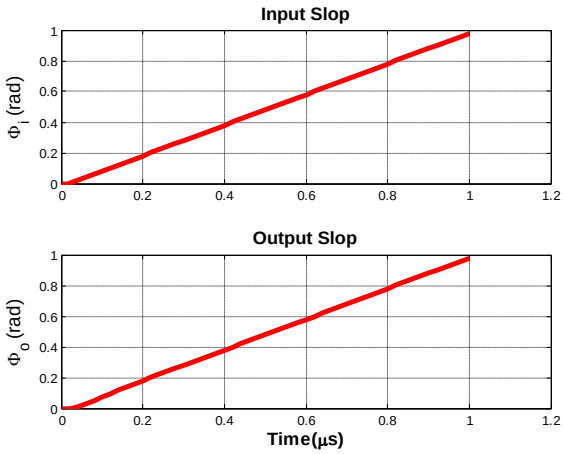

Figure 8. Output simulation by input slope

The waveform of the control voltage is shown in figure 9.

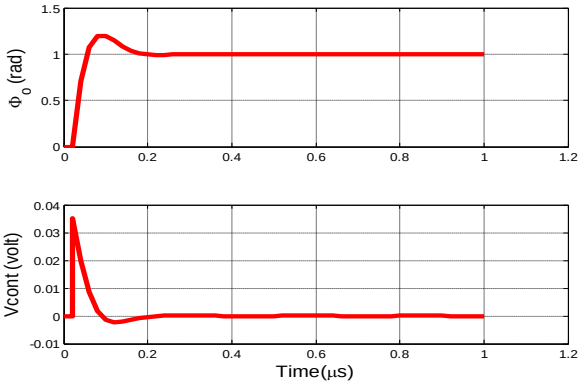

Figure.9. the waveform of the control voltage

A.**The design process**

According to the system stability, the value of ζ and PM is known and also generally consider ω_h=2MHZ in the circuits, and according to the VCO structure, the Kvco is known and by the value of ζ and ω_h the value of ω_n is obtained, and by known the value of ω_n, Ip is consider and by choosing Cp:

$$\left.\begin{array}{l} PM \rightarrow R_P C_P \omega_{PM} = R_P C_P \dfrac{R_P I_P K_{VCO}}{2\pi} \\ I_P, K_{VCO} \rightarrow known \end{array}\right\} \Rightarrow R_P \quad (16)$$

For analysis of transient behaviour, calculate the lock time and transient time ($\Delta\varphi$) of PLL plot it. Setting time or lock time is the time that the system response stays at certain range of final value. Figure 10 is shown the simulated output of phase-locked loop. Setting time or in other word, lock loop time is calculated as follows:

$$t_s = \frac{4}{\xi\omega_n} \quad (17)$$

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$$\xi\omega_n = \frac{1}{2} R_p \frac{I_p K_{VCO}}{2\pi} \quad (18)$$

since the value of Kvco, Ip and Rp is as follows: Kvco=100e6, Ip=260e-6, Rp=25.85e3, by placement above value in equation 13, the value of ξωn is equal to 5.35e005 which by putting these amounts in equation (16), the value offsetting time (lock time) is obtained which is the same amount of 7.47us that is obtained in the following plot.

B. **The calculation of the transient time ($\Delta\varphi$)**

To calculate must the transient time of both input wave from (reference) and phase-locked loop waveforms calculated and then subtract these two values of transient time to get a same value and plot it. Figure 10 is shown the sinusoidal input wave from (reference) diagram and the phase-locked loop waveform. The collision of both wave from to x-axis has a certain time, note these value and placement at the following equation which given the amount of transition time for each figure individually through it.

$$\Delta\omega = \omega * \Delta T \quad (19)$$

$$\omega = 2 * p_i * 10^6 \quad (20)$$

Figure 10 is shown the transition time diagram, as shown in the figure, in time 7.47 us, the transition time comes to zero which indicates the phase difference value of input and output of phase-locked loop and fast lock is calculated properly.

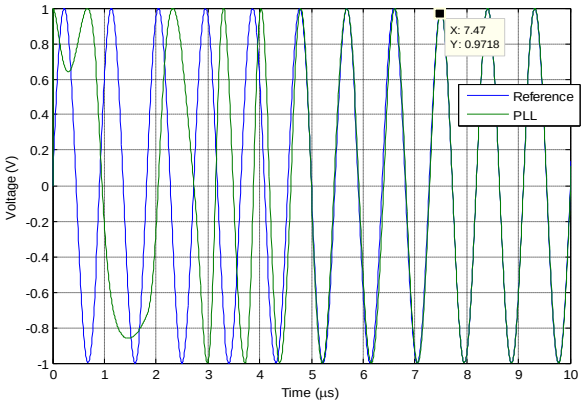

Fig 10.PLL output and locks time

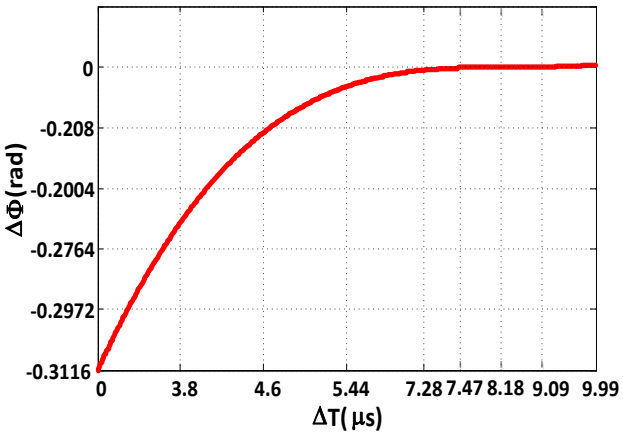

Fig 11.transiant time diagram

C. **The investigate of each parameters of loop effects in fast lock at phase area**

In this section, the effect of each parameters of loop on the fast lock investigated and draws the relevant diagrams. If increase the value of current Ip, the fast lock of phase-locked loop decreased and the fast lock increased, the overshoot value increase (the output peak increases) and both sides of the peak add the output wave from closer together and so gradually, the value of overshoot (peak) is reduced and the output going to delete the peak and this continues where the current is 550 us and after that the output peak completely removed and the output wave from does not change ,if increase the current value the output will not change, that means at the current 615 us and after that the output goes to out of lock situation and in 625 us the output is completely removed from lock situation and lose ideal state and the stability increase if reduce the value of current Ip , means less that 100uA , by reduces the current, the value of overshoot in output waveform increase and lock time increase and the fast lock of loop decreased this is where that choose the current 20uA , will lose ideally situation of output waveform and removed from the lock state completely and stability reduced which is shown in figure 12.

D. **The effect of changing the value of resistance**

By increase the value of resistance, fast lock decreased and in other word lock time increased and the overshoot is going to decrease and the output goes to remove the overshoot and the stability increases. if the resistance value less than 2.2 k , the loop lock time increase slowly and the fast lock decrease , the overshoot increase, the stability reduce and the output goes to out of lock situation , and at 500 resistance the overshoot and output wave from disappears. And by reduce the resistance value gain, the ring is slowly unlocked so that at 535 resistance, the loop completely removed at lock situation which output is shown in figure 13.

E. **The effect of changing the value of capacitance**

By increase the value of capacitance, the value of overshoot decrease gradually and goes to fading, unit at 70uF, there is no overshoot and the curved convert to the line, fast lock increased and lock time decreased and after the certain value (500 nF),no changes is created in the output wave form and by reduce the capacitance value , lock time increased and lock speed decreased and also the value of overshoot in output in increasing, so that at 0.1nF the waveform completely removed at lock situation that is shown in figure 14.

F. **The effect of changes in gain value of voltage controlled oscillator (kvco).**

By increasing the value of kvco, the loop lock time decrease and fast lock increase and also the overshoot of output waveform is decreasing slowly.by reducing the value of kvco, the ring lock time increase and the fast lock decrease and the overshoot is increasing and at 40mhz the loop removed at lock situation completely which is shown at figure 15.

If we want to change the value of all loop parameters at the same time, due to the complexity of equations, analysis and design is not easy to achieve the desired characteristics.

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Table 2. The effect of loop parameters at fast lock

		Lock Time	Fast lock	Overshoot	Stability
Ip	↑	↓	↑	↓	↑
Ip	↓	↑	↓	↑	↑
R	↑	↓	↑	↓	↑
R	↓	↑	↓	↑	↓
C	↑	↑	↓	↓	↑
C	↓	↑	↓	↑	↓
Kvco	↑	↓	↑	↓	↑
Kvco	↓	↑	↓	↑	↓

IV. **Conclusion**

One of the phase-lock the loops challenges where studied in this paper is calculated the lock time to this end , the phase lock loop at system level (phase model) and circuit level to check the function of it is simulated and then the transition time is calculated and the effect each loop parameters on the fast lock is investigated and by compare the results of the proposed equation with simulation results to evaluate the presented equations the following results were obtained by increasing the charge pomp current and voltage controlled oscillator gains, the loop lock time reduced but by reducing the resistance value and increase and decrease of capacitance value and reduce the voltage controlled oscillator value the lock loop time is increases .as we can designed the lock loop phase in the shortest possible time, which the input and output frequency be equal together and the difference between input and output phases to certain value (close to zero).that means we could reduce the lock time and increase the fast lock and also consider the stability, phase noise and jitter .

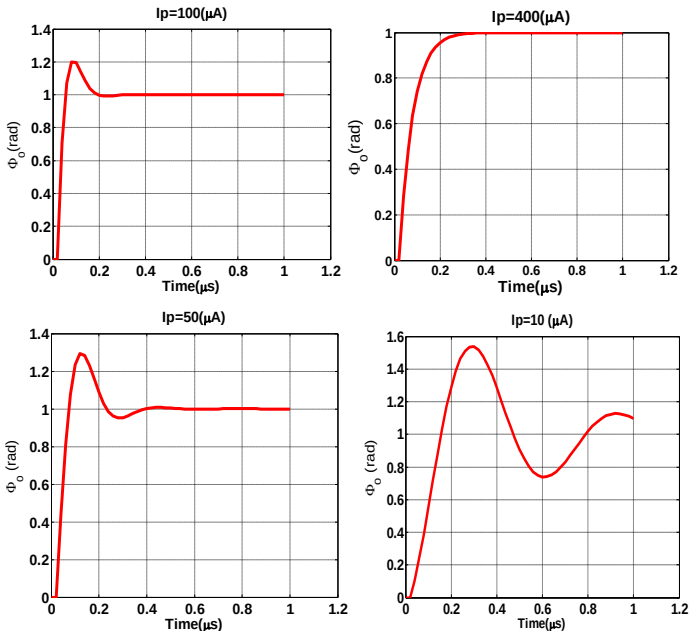

Fig 12. The increase and decrease of current Ip

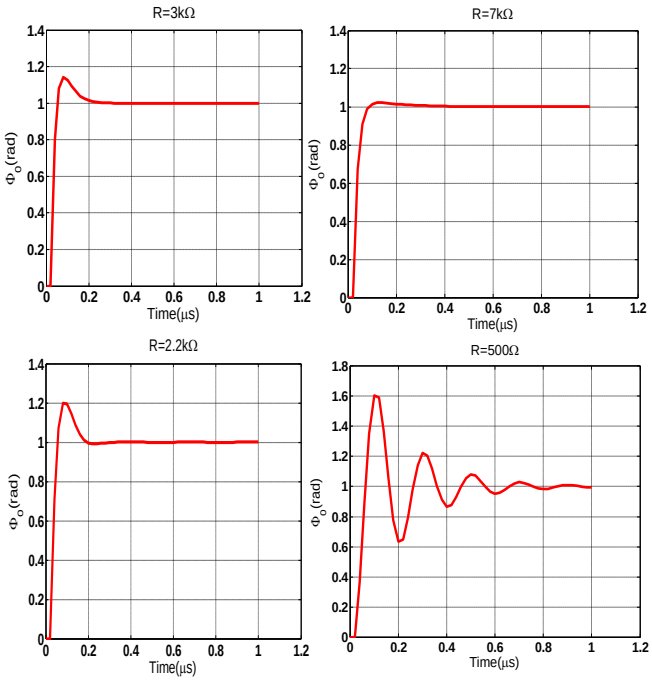

Fig 13.increase and decrease of resistance value

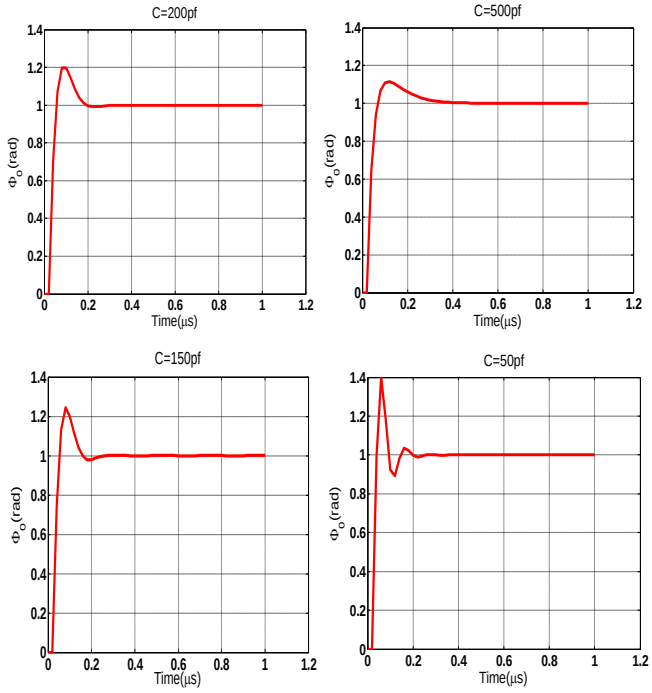

Fig 14. Increase and decrease of capacitance value

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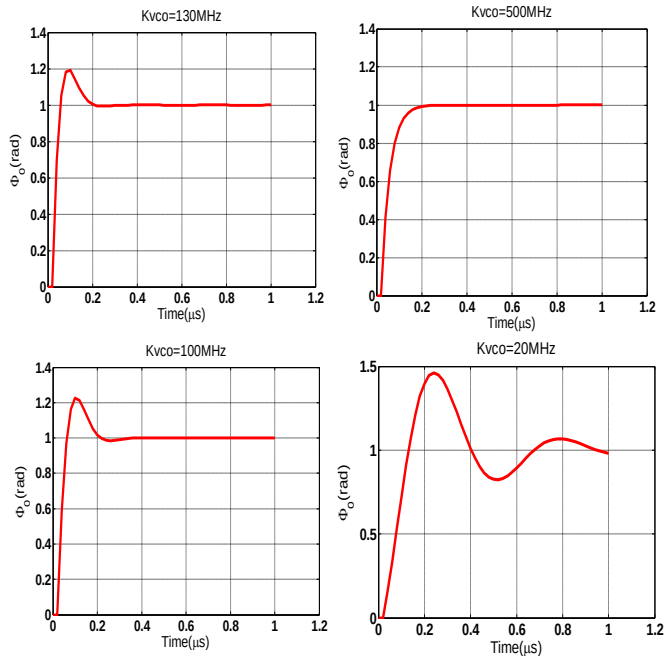

Fig 15. Increase and decrease of Kvco

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